The Sandbridge Sandblaster SB3000 Multithreaded CMP Platform

John Glossner, Ph.D., Co-Founder, CTO & EVP

jglossner@SandbridgeTech.com

1 North Lexington Ave, 10th Floor
White Plains, New York 10601
914-287-8500

Agenda

Sandbridge Introduction
- Company Background
- Motivation

Sandblaster Platform
- ISA
- Vector Architecture
- Multithreading
- Saturating arithmetic

Hardware
- Low Power Core
- SB3000
- RF

Software
- IDE
- Compiler
- Simulator

Communications
- WCDMA, GPRS
- GPS
- 802.11b

Applications
- H.264 / MPEG4
- MP3

Summary

Sandbridge Technologies

Fabless Semiconductor Company

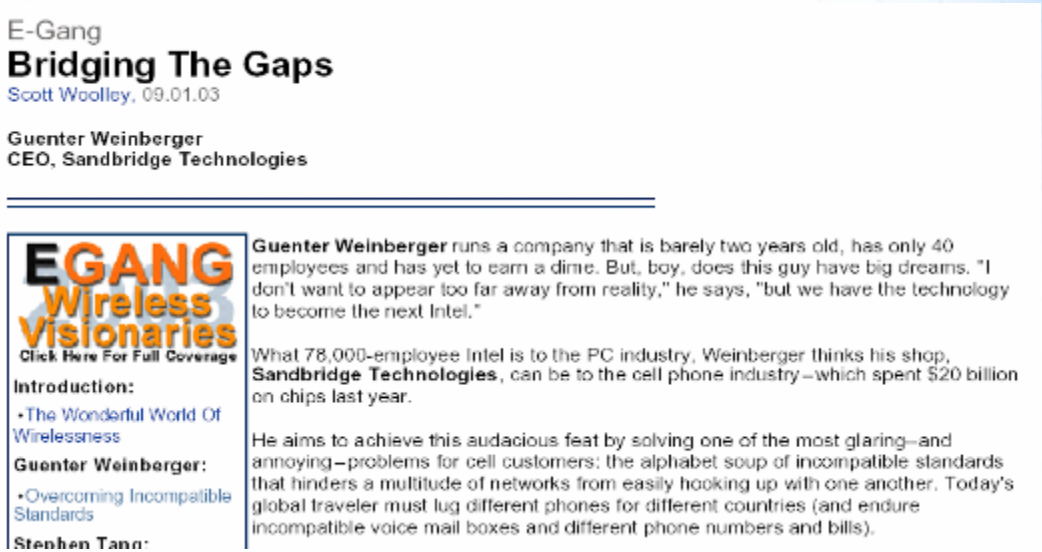
developing…

Software reconfigurable

Wireless chipsets for low power applications

WORLD ECONOMIC FORUM

COMMITTED TO IMPROVING THE STATE OF THE WORLD



E-Gang

Bridging The Gaps

Scott Woolley, 09.01.03

Guenter Weinberger
CEO, Sandbridge Technologies

EGANG Wireless Visionaries

Click Here For Full Coverage

Introduction:

•The Wonderful World Of Wirelessness

Guenter Weinberger:

•Overcoming Incompatible Standards

Stephen Tang:

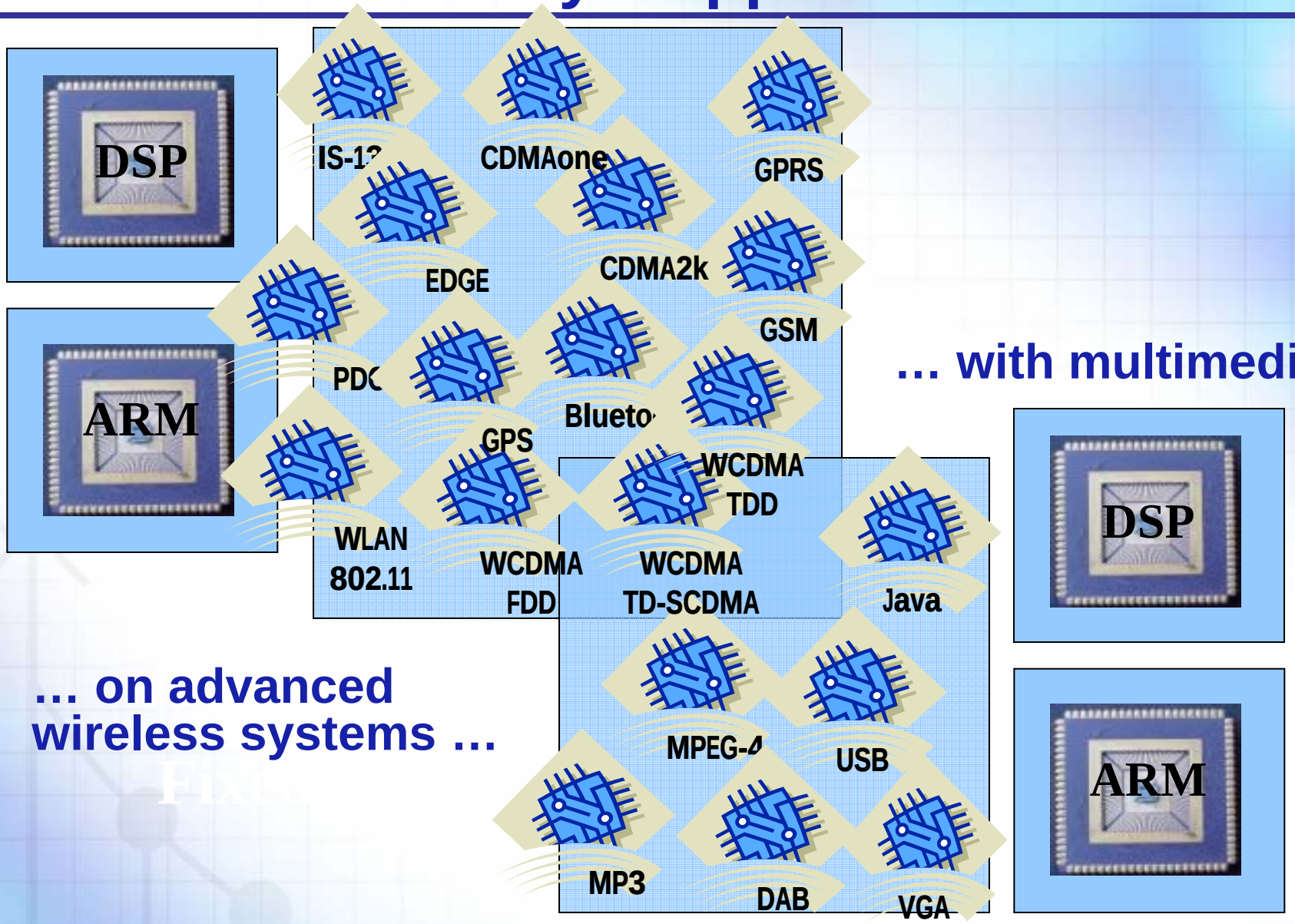
Guenter Weinberger runs a company that is barely two years old, has only 40 employees and has yet to earn a dime. But, boy, does this guy have big dreams. "I don't want to appear too far away from reality," he says, "but we have the technology to become the next Intel."

What 78,000-employee Intel is to the PC industry, Weinberger thinks his shop, **Sandbridge Technologies**, can be to the cell phone industry—which spent $20 billion on chips last year.

He aims to achieve this audacious feat by solving one of the most glaring—and annoying—problems for cell customers: the alphabet soup of incompatible standards that hinders a multitude of networks from easily hooking up with one another. Today's global traveler must lug different phones for different countries (and endure incompatible voice mail boxes and different phone numbers and bills).

SANDBRIDGE TECHNOLOGIES

A Whole Industry's approach failed …

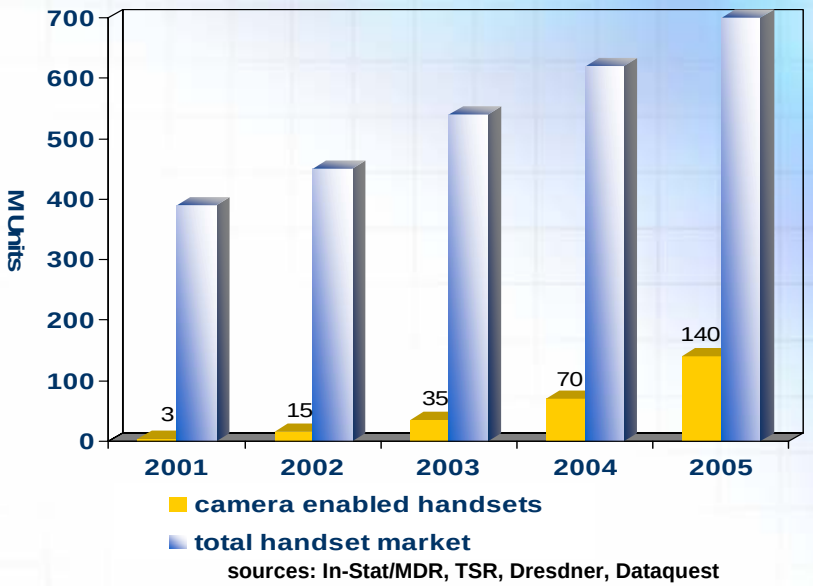


… with multimedia

… on advanced wireless systems …

SANDBRIDGE TECHNOLOGIES

What is it that we eventually carry with us ?

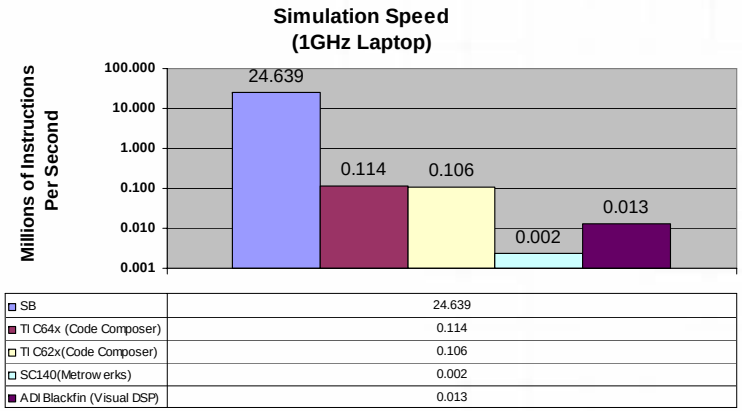


It has a color screen, camera, audio and antenna …
… but all features need high computing performance and ultra low power consumption

- **Wireless communication 2G – 2.5G – 3G – WLAN – BT – etc.**
  - GSM/IS-95a,b/IS-136/PDC/ iDEN – CDMA2k/GPRS/EDGE – FDD/TDD/TD-SCDMA/Jap.WCDMA/CDMA2k-3x– 802.11a,b,g
- **Radio broadcast GPS – radio – TV – etc.**
  - Location based services/911/tracking services – AM/FM/DAB – Sat./Terr.TV
- **Encryption – decryption – media encode – media decode**
- **Games – speech to text – natural language processing**

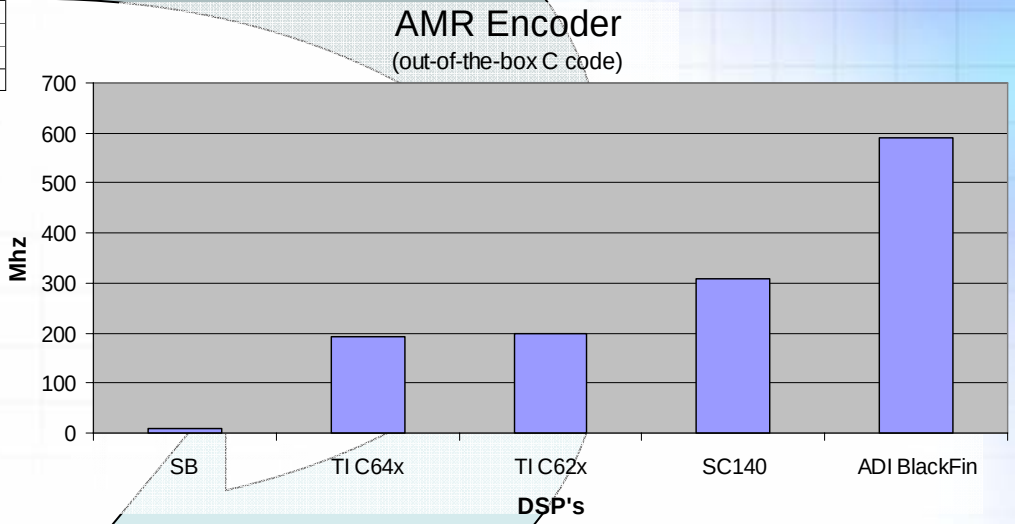
SANDBRIDGE TECHNOLOGIES

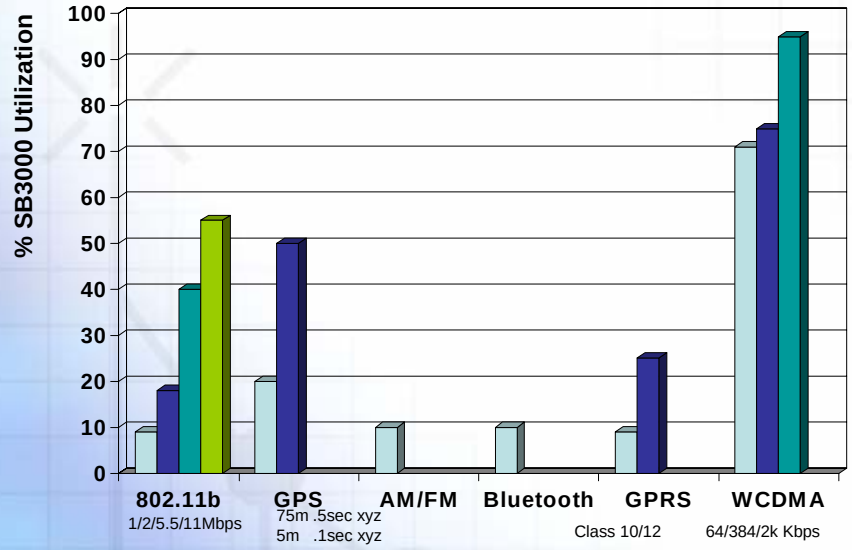
Handset design at C level in min. time



Complete system design in C

- Cycle accurate simulator delivers immediate feedback
- Design for conformance in C





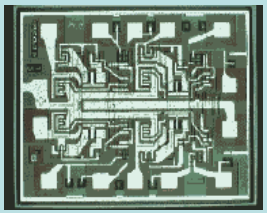
System performance by design

- Parallelizing compiler generates production assembly code
- Multithreading (sea-of-threads) ensures concurrent execution

SANDBRIDGE TECHNOLOGIES

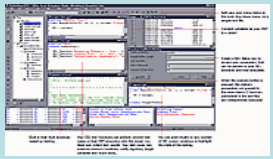
The Sandbridge Approach …

SandBlaster™ DSP



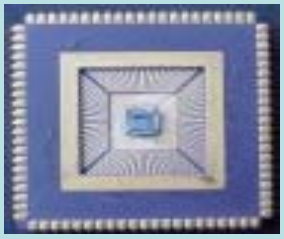
- Programmable
- Ultra-low power
- High-performance
- Multithreaded

SandBlaster™ Tools



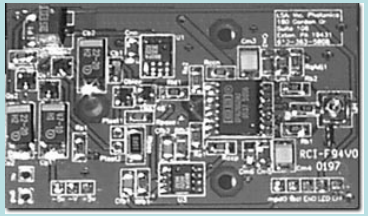
- Improved productivity C compiler
- 70% reduction In time-to-market
- User-friendly

DSP Platform



- Scalable & Programmable
- Integrated Sandblaster cores
- Up to 2Mbit/sec data rate
- 40,000 RISC MIPS
- Low Cost 0.13um CMOS
- Integrated protocol stack

DSP Ref Design



- Low Cost
- Power Efficient
- Ultra-high performance
- Fully tested / validated
- Dedicated Customer Support
- Flexible and upgradeable

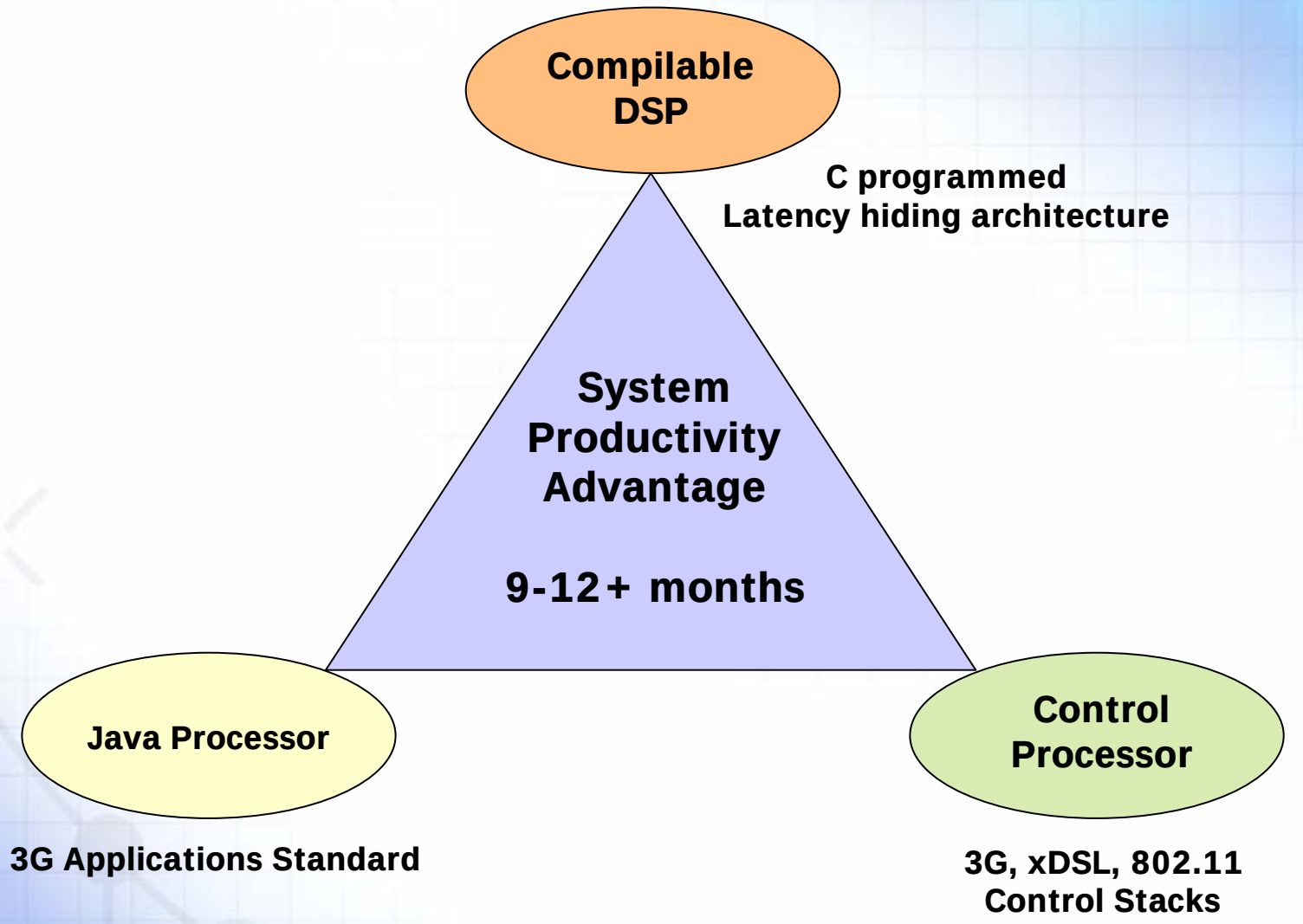
Core technology equally applicable to Networking, Storage, Automotive, GP-DSP, etc.

SANDBRIDGE TECHNOLOGIES

Architecture

SANDBRIDGE TECHNOLOGIES

Sandblaster Architecture Performs



SANDBRIDGE TECHNOLOGIES

Multithreaded Architecture Enables C

Key to Low Power Implementation

Code&Data Sharing Across Threads

Sea of Threads

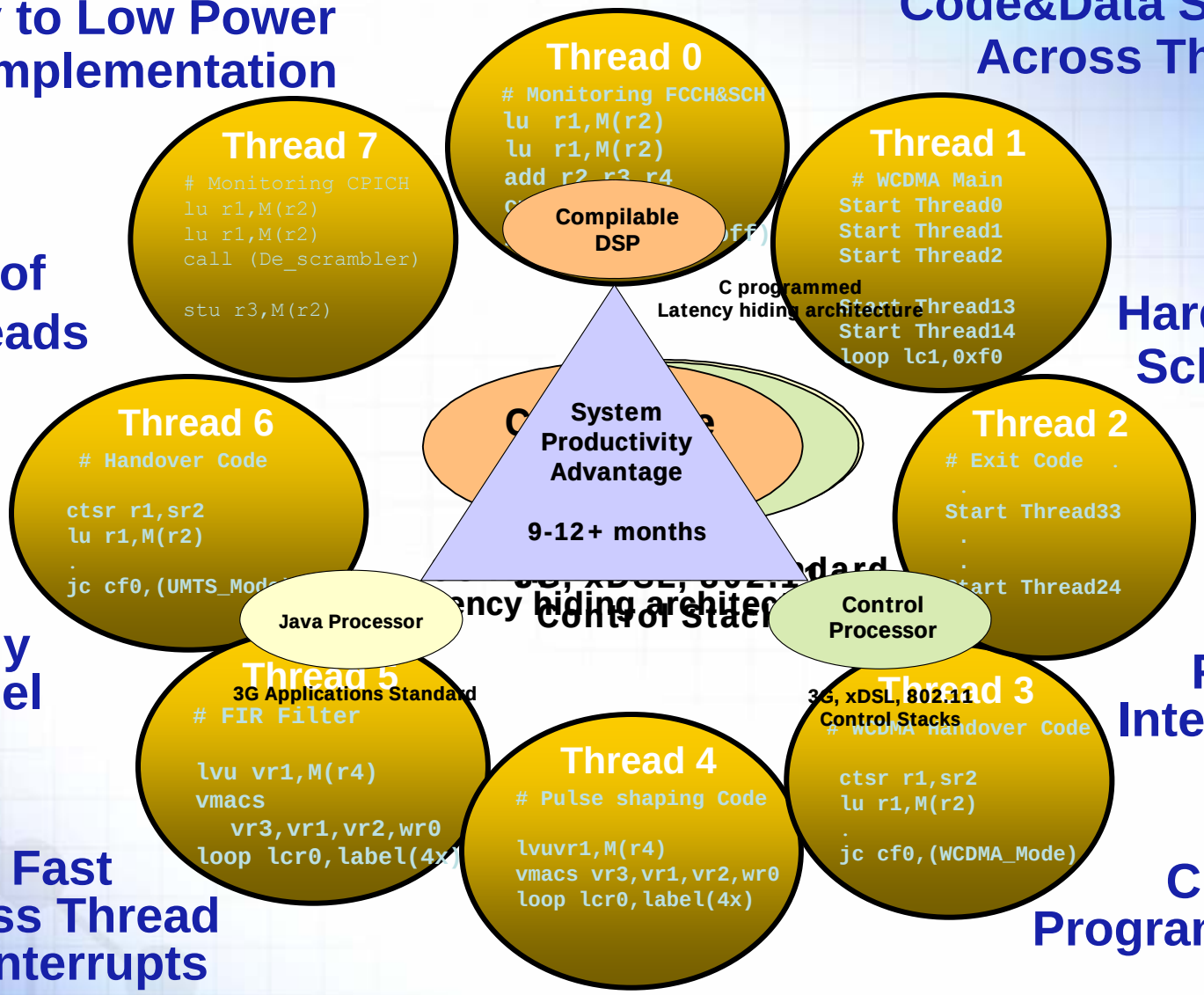
Hardware Scheduled

Highly Parallel

Fully Interlocked

Fast Cross Thread Interrupts

C Programmed



SANDBRIDGE TECHNOLOGIES

Parallelism

Multiple cores (MP)

- 4 cores

Multithreaded (TLP)

- 8 threads/core

Compound Instructions (ILP)

- 3 operations out of
  - Integer
  - Load/Store
  - Branch
  - Vector

Vector (DLP)

- 4 data parallel operations

Performance

Peak

- 3 operations/cycle
- 16 RISC-ops/cycle
- 4 MACS/cycle

Example

```
L0: lvu %vr0,%r3,8
||  vmulreds %ac0,%vr0,%vr0,%ac0
||  loop %lc0,L0
```

- load vector update: 4 16-bit loads + address update
- vector multiply and reduce: 4-16 bit saturating multiplies + 4 32-bit saturating adds
- loop: decrement, compare against zero and branch

20 tap FIR

- 3.92 taps/cycle sustained including automatic multithreading
- ~16 RISC-ops/cycle sustained

Saturating Arithmetic

Many DSP applications require saturating arithmetic

Saturation means

- Results greater than largest representable number are saturated to the largest representable number
- Results less than the smallest representable number are saturated to the smallest representable number

- 4-bit precision example:

```
   A =   0.101 = 0.625        A =   1.011 = -0.625
+  B =   0.111 = 0.875     +  B =   1.001 = -0.875
=  S =  01.100 = 1.5       =  S =  10.100 = -1.5
S|   =   1.100 = -.5       S|   =   0.100 = +.5
<S>  =   0.111 = 0.875     <S>  =   1.000 = -1.0
```

Saturating Arithmetic (2)

Saturating arithmetic operations are not associative

4-bit precision example

```
<<<-1.0*-1.0> + <0.5*0.5>> + <-0.5*0.5>>
    = <<0.875 + 0.25> - 0.25>
    =    0.875          - 0.25          = 0.625
```

```
<<-1.0*-1.0> + <<0.5*0.5> + <-0.5*0.5>>>
    = <0.875 + <0.25-0.25>>
    =  0.875 +       0                 = 0.875
```

Sandbridge Low Power Hardware

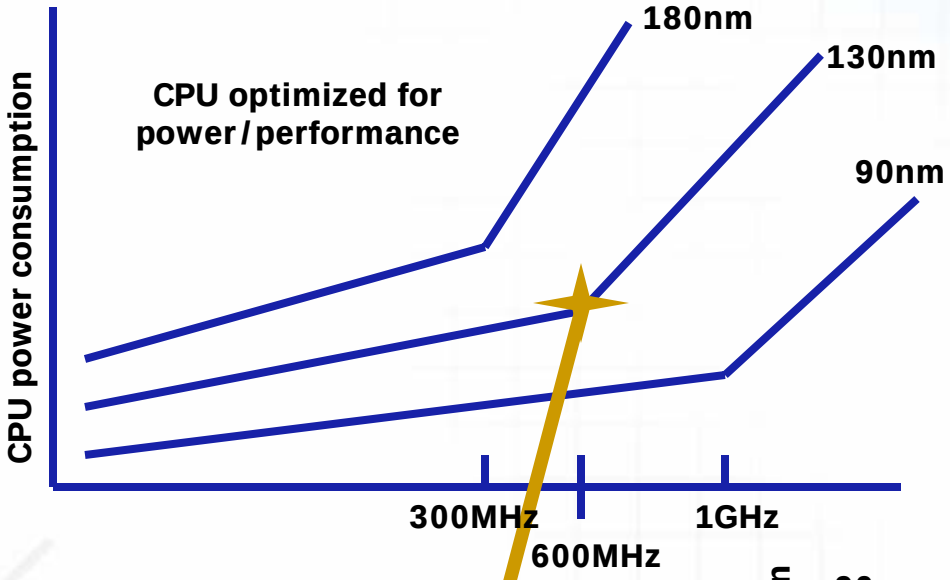
SANDBRIDGE TECHNOLOGIES

Low Power IDLE Instructions

Architecturally possible to

- Turn off 1 or more processors
  - All clocks disabled
  - Instruction fetch disabled
  - Memory disabled
  - Memory state not preserved
- Turn off 1 or more threads within a processor
  - Clocks disabled on a per thread basis
  - Instruction fetch disabled on a per thread basis
  - Memory state preserved (including registers)
  - Threads awaken via interrupt

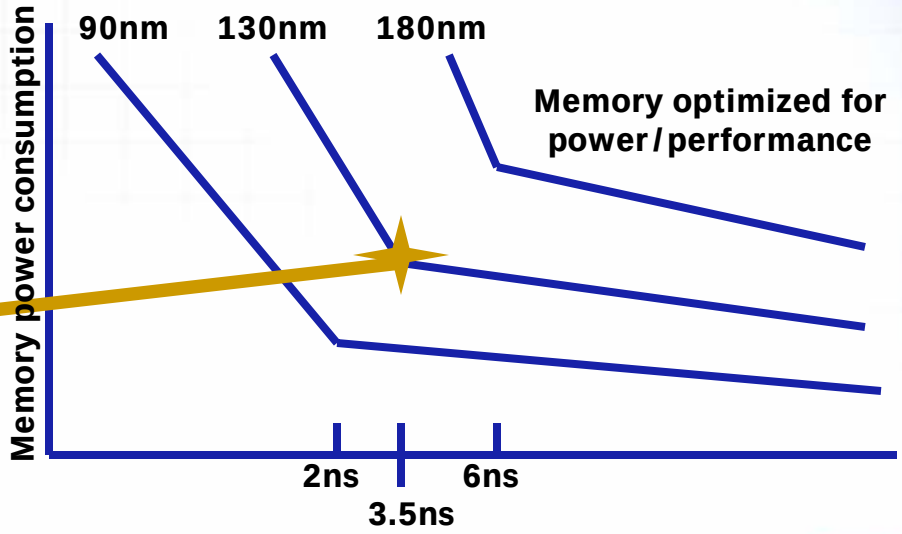
Using Multithreading to Optimize for Power



- Multiple cycles to access memory
- Slow memory accesses hidden by multithreading

Multithreading decouples CPU from MEM, combining best power/performance for CPU AND MEM

- Optimized CPU power
- Optimized memory power
- Optimized overall power/performance



SANDBRIDGE TECHNOLOGIES

SandBlaster Pipeline

	0	1	2	3	4	5	6	7	8	9	10
Ld/St	Inst Dec	RF Read	Agen	Xfer	Int. Ext	Mem 0	Mem 1	Mem 2	WB		
ALU	Inst Dec	Wait	RF Read	Exec1	Exec2	Xfer	WB				
I_Mul	Inst Dec	Wait	RF Read	Exec1	Exec2	Exec3	Xfer	WB			
V_Mul	Inst Dec	RF Read	MPY1	MPY2	Add1	Add2	Xfer	WB			
V_Mul Reduce	Inst Dec	RF Read	MPY1	MPY2	Add1	Add2 RF Rd	Reduce 1	Reduce 2	Reduce 3	Reduce 4	WB

Staggered Read/Write

- Allows single write-port register files

Very Long Reduce

- Shifted/Offset against vector pipe

Interlock Checking Hardware

The multithreaded implementation is transparent

- No interrupt restrictions
- Load / Branch delay slots not visible

Multithreading hides instruction execution latencies

No interlock checking hardware is required

- One exception – long loads

Single Register File Write Ports

A single compound instruction can contain a vector load or store and a vector operation.

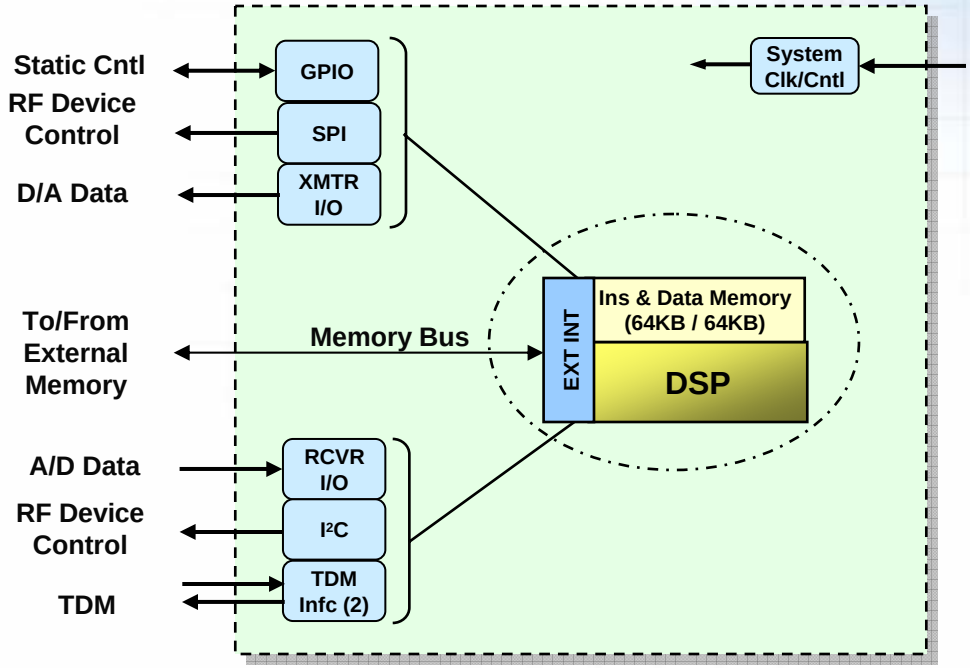
```
stvu    %vr1, r0, 8 || vmac %vr5, %vr4, %vr3, %ac0
```

- Our design requires a single write port per space
  - int 1R/1R, vec 2R/1W, and acc 1R
- VLIW's may require 14R/5W for the same computation
- If load, up to 9W simultaneous write ports may be required

Our design staggers Load/Stores in multiple ways:

- Time staggered
  - different pipeline stages
- Spatially staggered
  - Banked register files
- Architecturally staggered
  - Separate architected register spaces (e.g. Integer, Vector, Accumulator)

SBTC 8/02

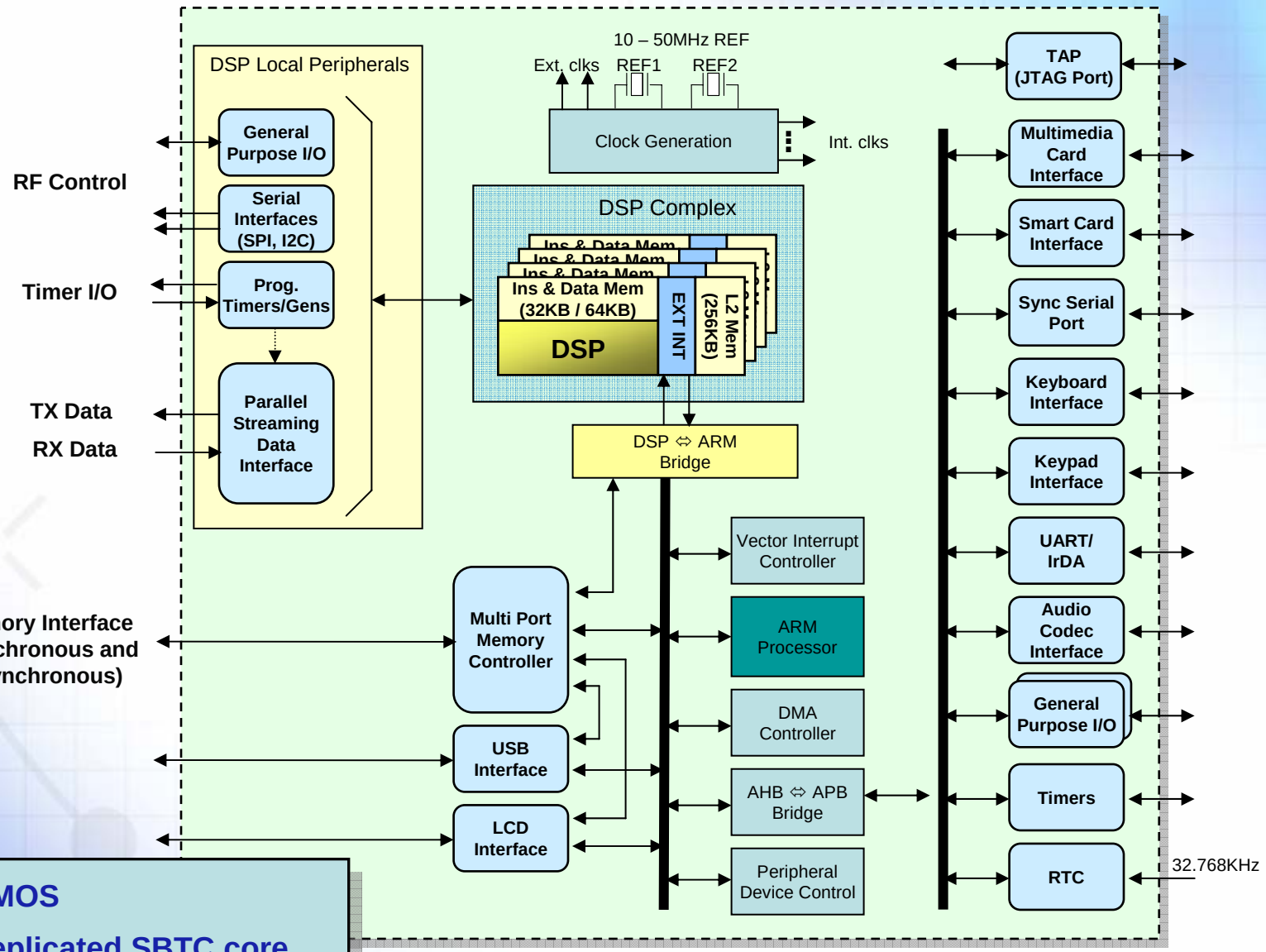


- 0.18um CMOS ASIC
- Single DSP Core
- SW Programmable
- External Bus for L2 memory
- Internal Inst/Data memory
- Control Interfaces: I^2C, SPI, TDM, A/D, D/A

SANDBRIDGE TECHNOLOGIES

SBTC Digital Card

SB3000 Handset Chip



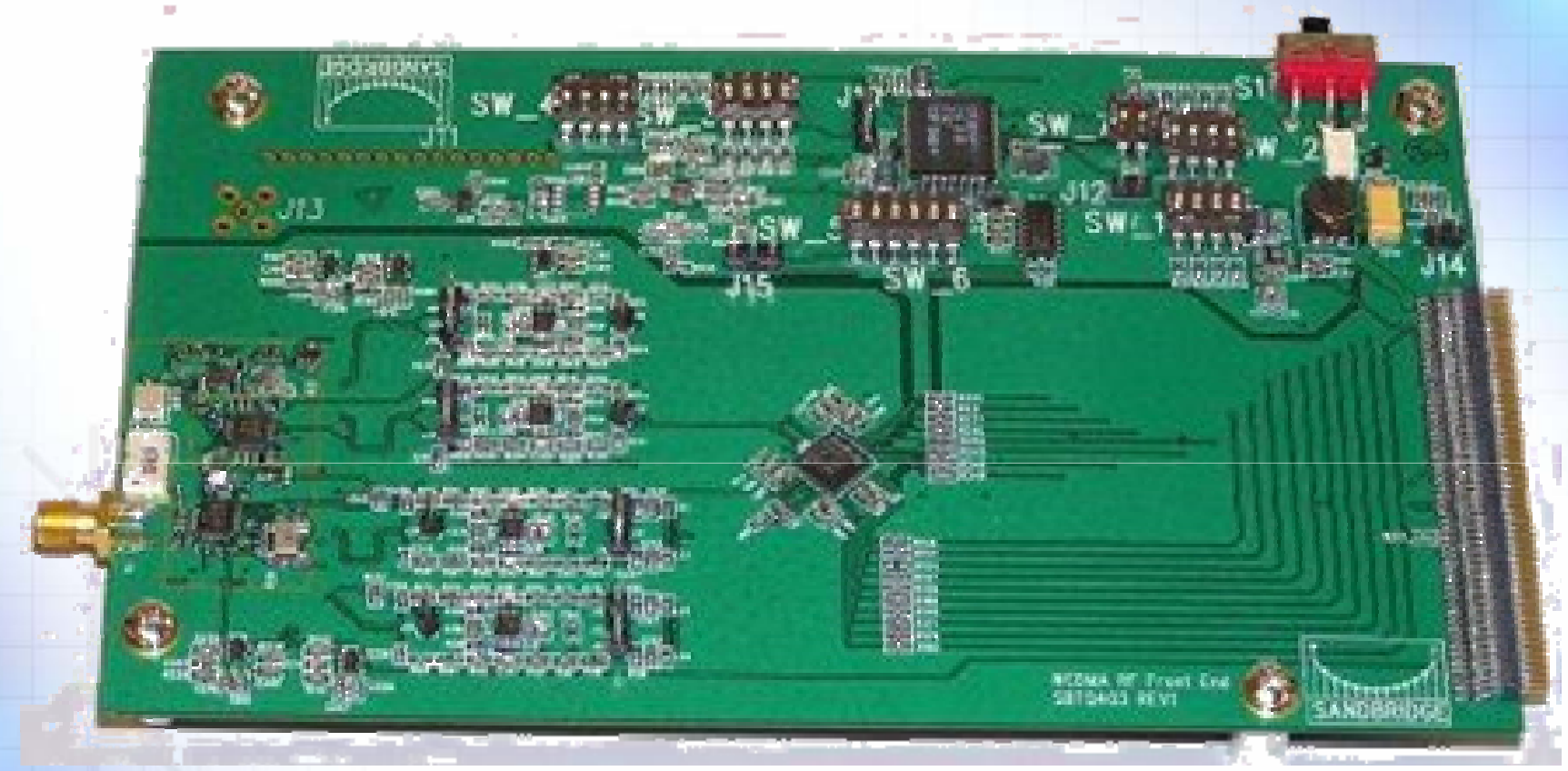
- CMOS
- Replicated SBTC core
- Low Power design

SANDBRIDGE TECHNOLOGIES

SB3000 Digital Card

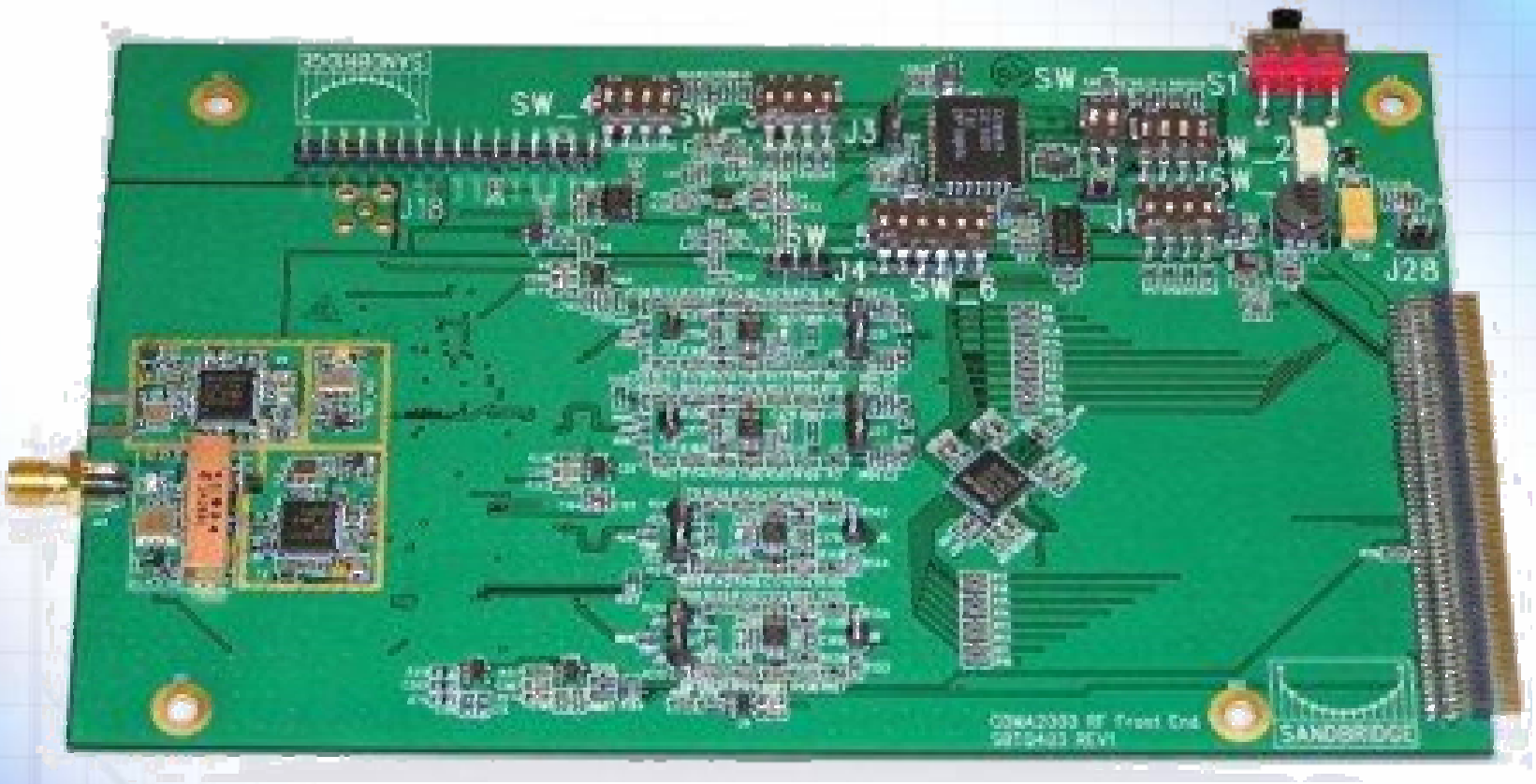
SANDBRIDGE TECHNOLOGIES

WCDMA 2Mbps Front End Card



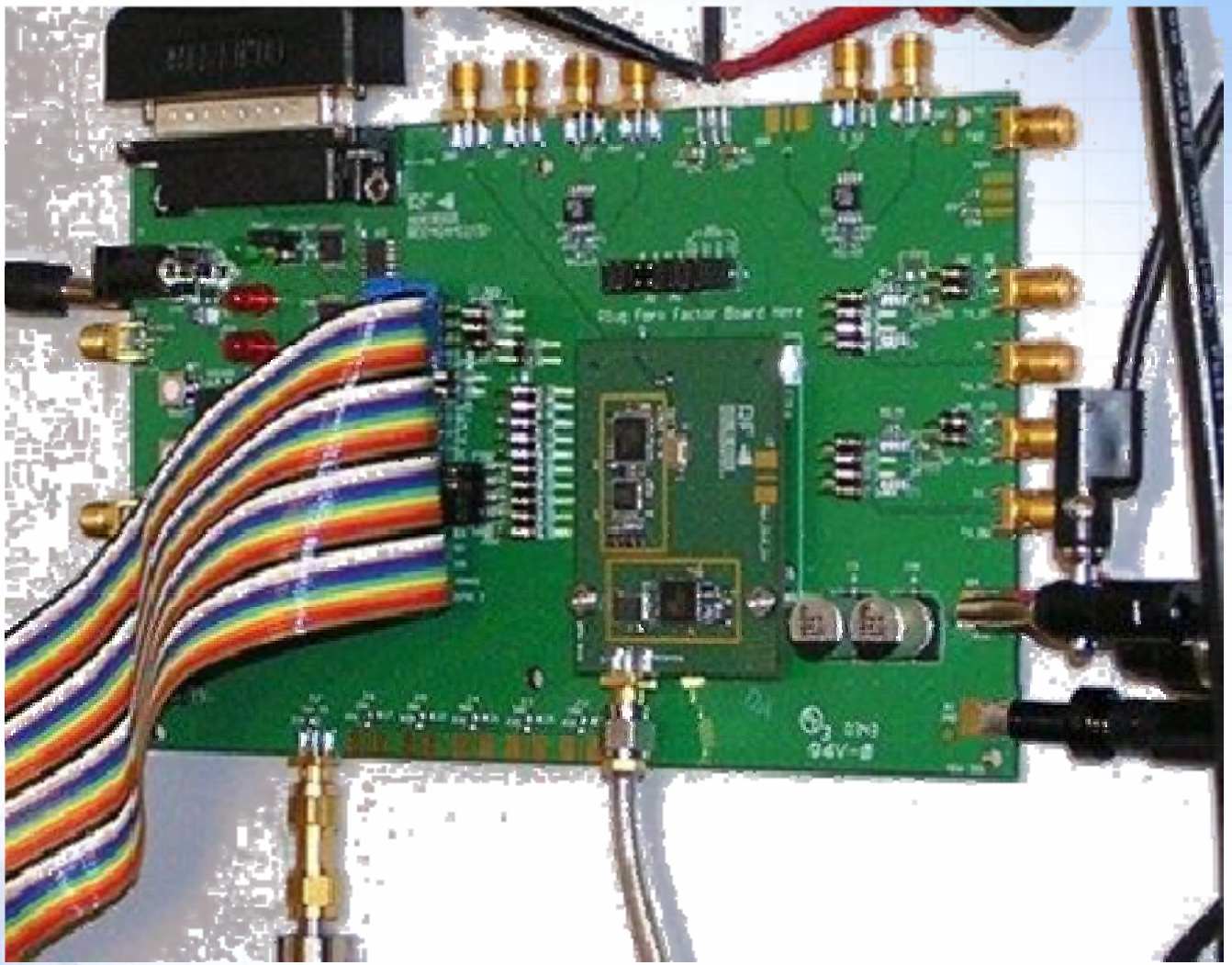
SANDBRIDGE TECHNOLOGIES

CDMA-2k Front End Board



SANDBRIDGE TECHNOLOGIES

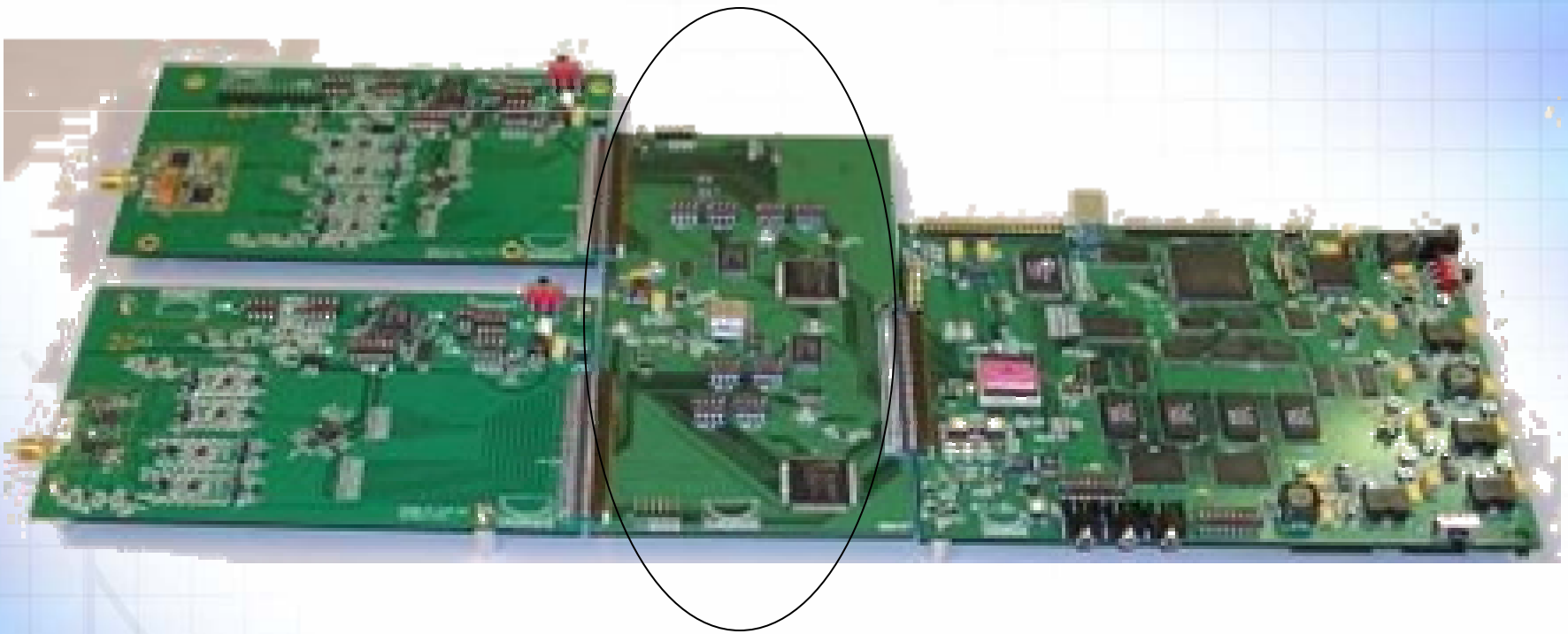
GSM/GPRS Front End Card



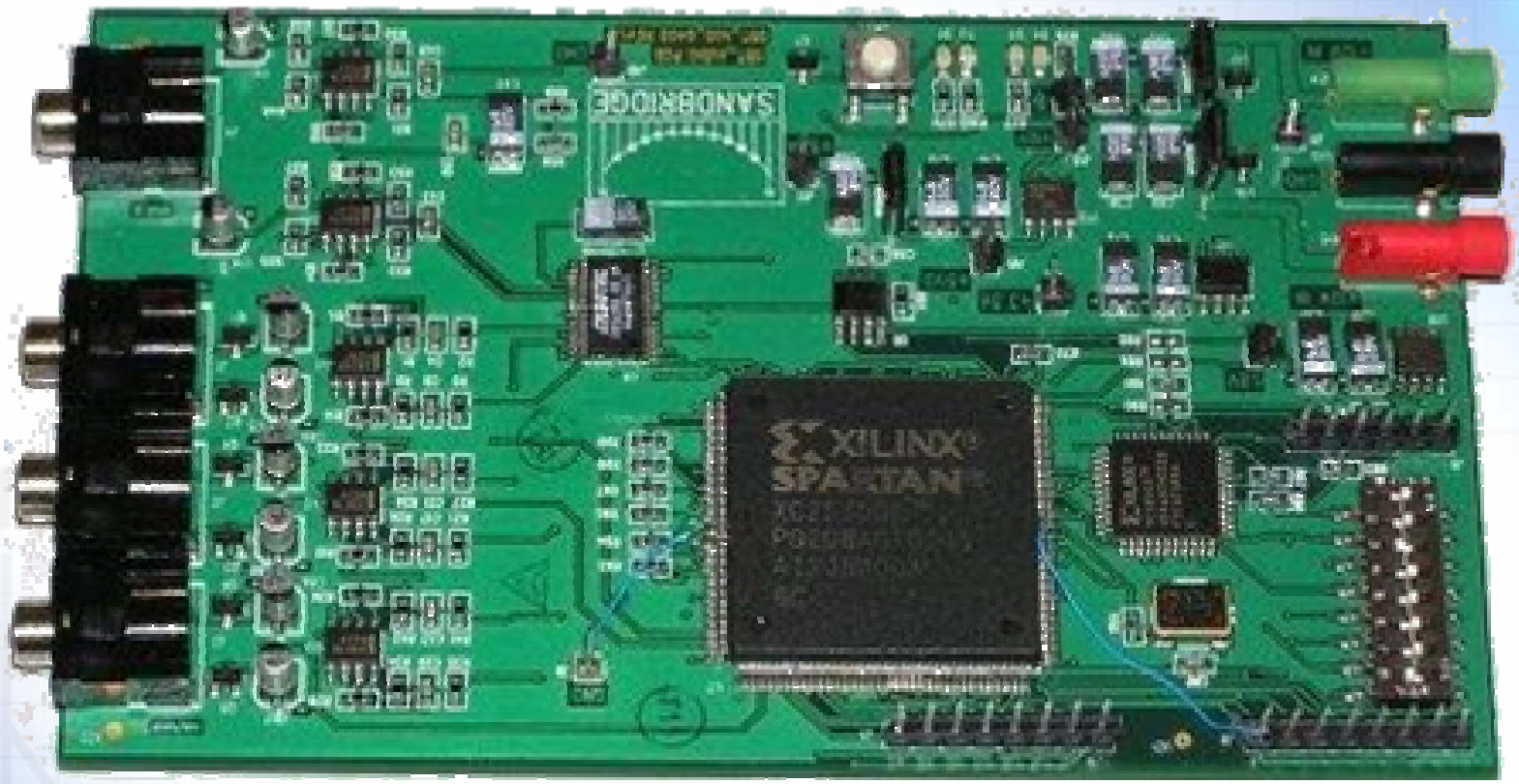
802.11b WLAN Front End

SANDBRIDGE TECHNOLOGIES

Multiplexer Board Block Diagram



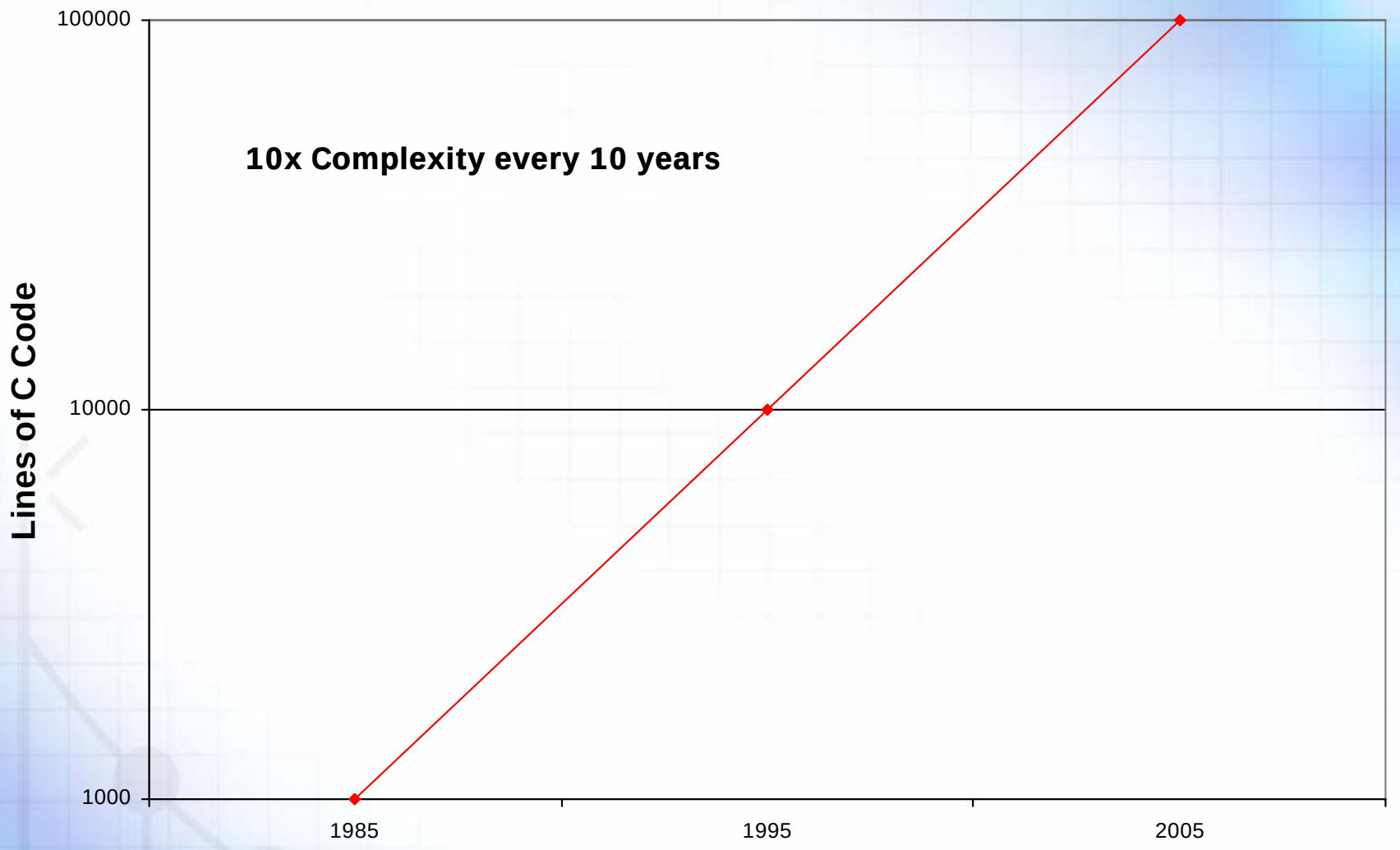
Audio Board



Sandbridge Software Tools

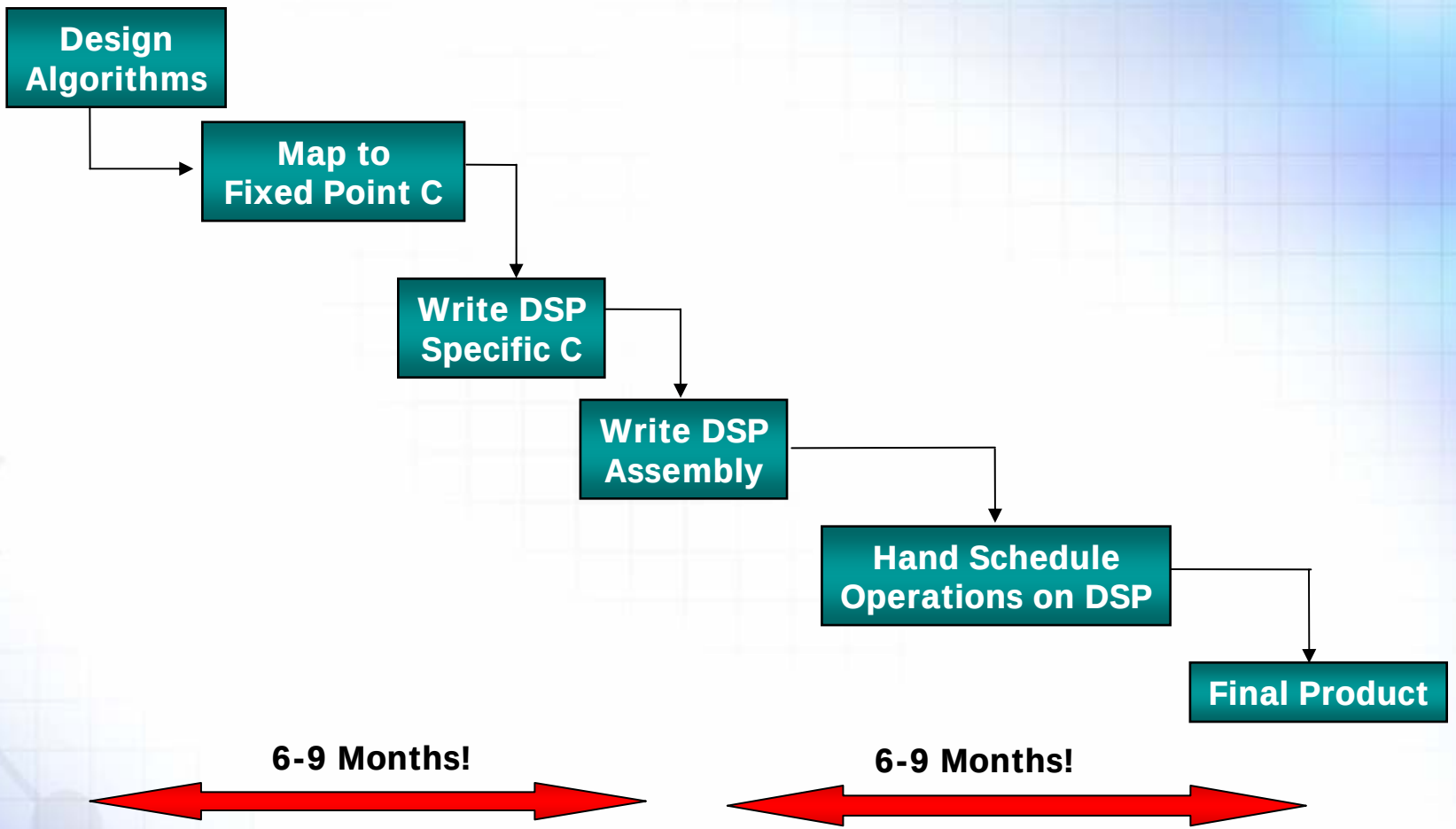
SANDBRIDGE TECHNOLOGIES

DSP Application Complexity



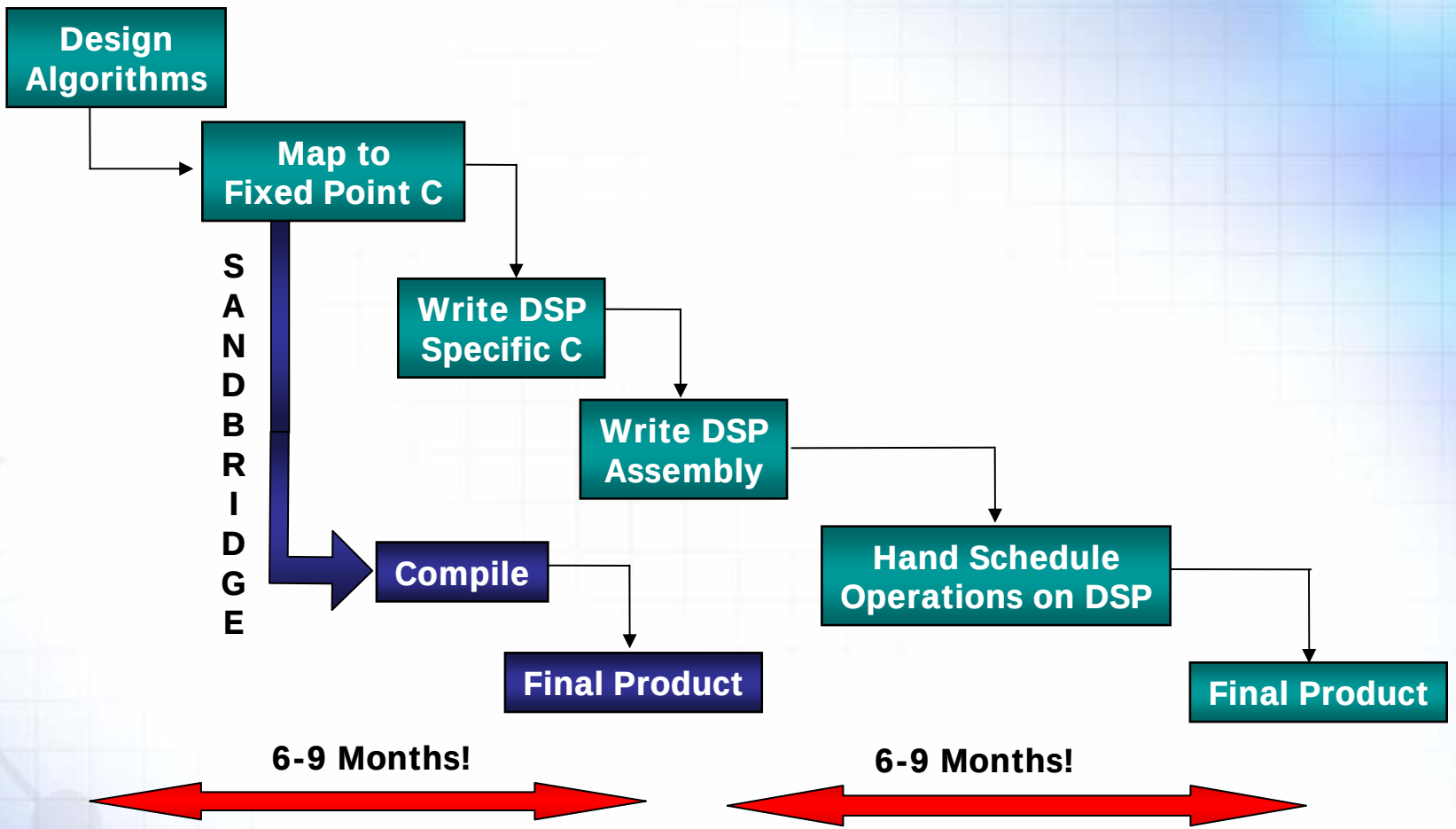
SANDBRIDGE TECHNOLOGIES

Compiler saves R&D and time-to-market …



SANDBRIDGE TECHNOLOGIES

Compiler saves R&D and time-to-market …



Sandblaster™ Provides Dramatic Improvement

SANDBRIDGE TECHNOLOGIES

System Software

Compilation Tools

- Compiler
- Assembler
- Linker
- Loader

Library

- C library
  - Standard C & Math
- Device drivers

Simulator

- Just-in-time
  - Models peripherals
- Cycle-accurate C
- Cycle-accurate VHDL

IDE

- Netbeans based
- Integrated S/W debug

RTOS

- Light-weight kernel
  - Based on POSIX API
  - Filesystem

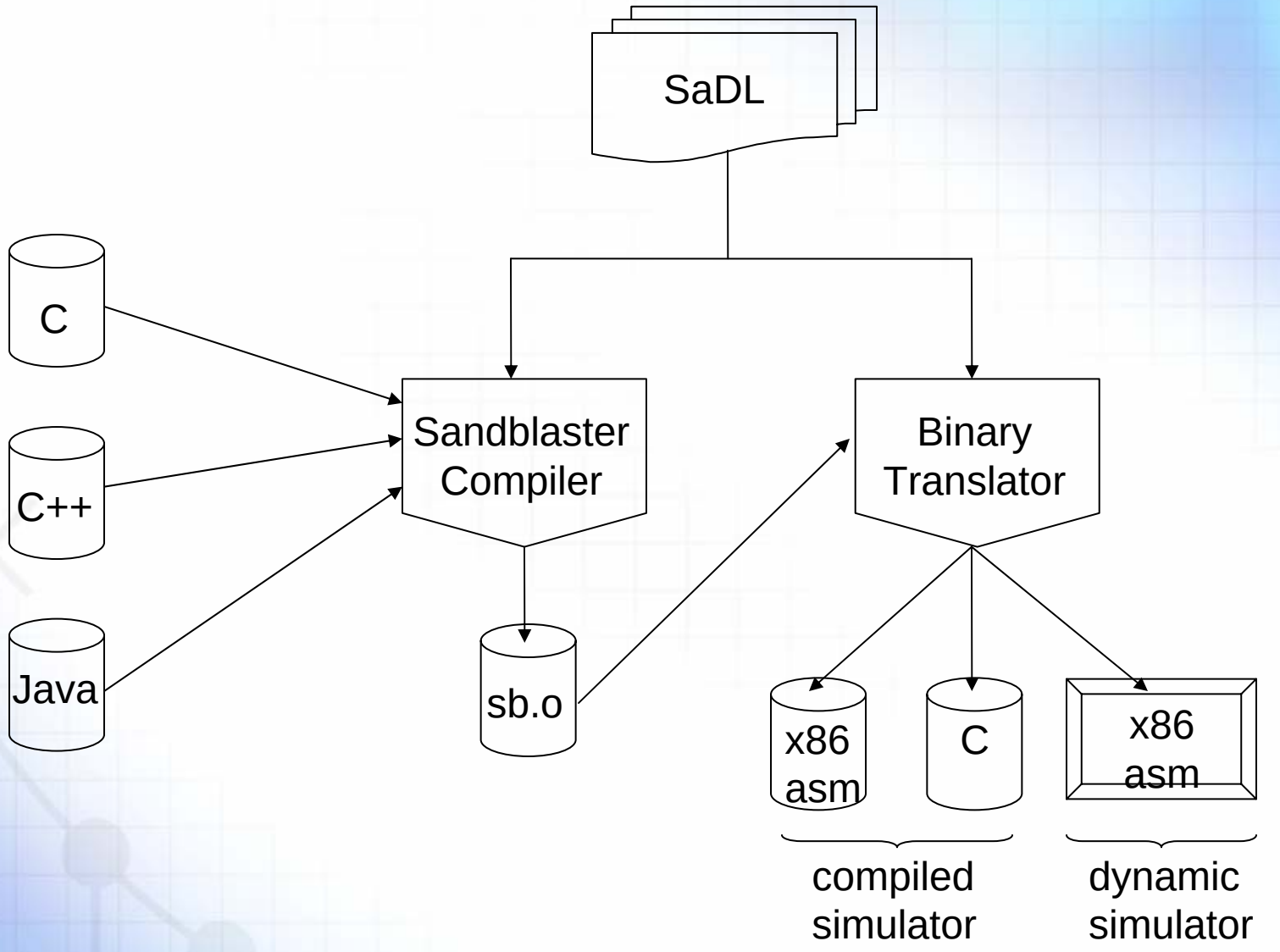
Test-Cases

- DSP kernels
- DSP applications
- Commercial test-suites
  - Plum-Hall, Perennial, Nullstone,CosY
- Nightly builds

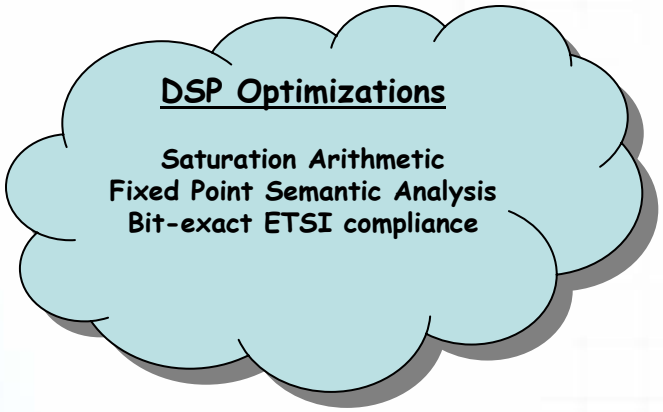
H/W Debugger

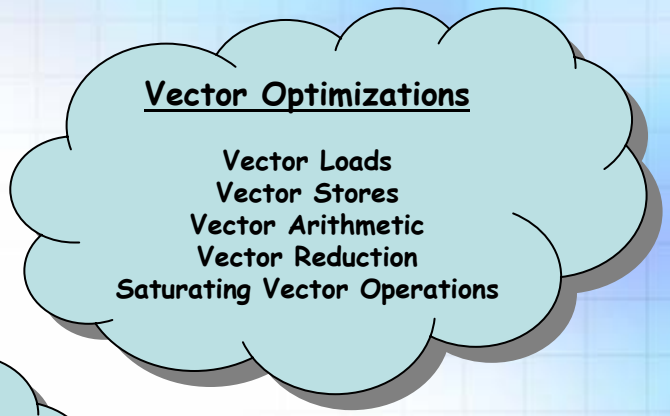
- Breakpoint/profile
- JTAG

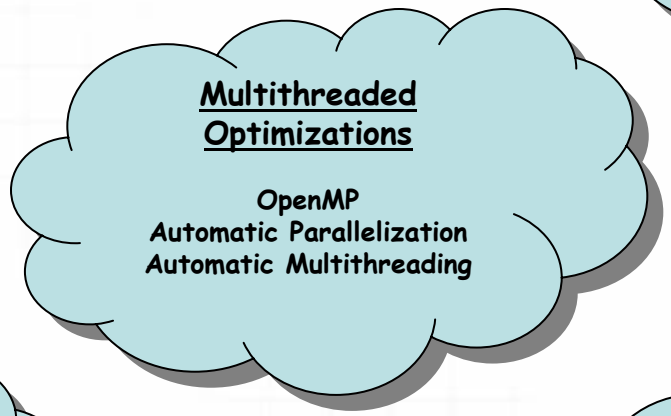
Sandblaster Tools

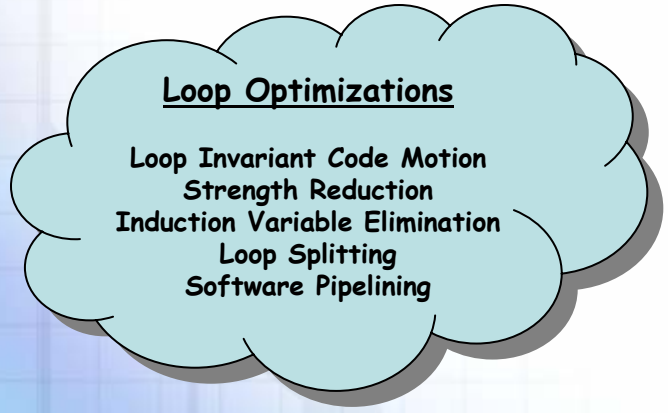


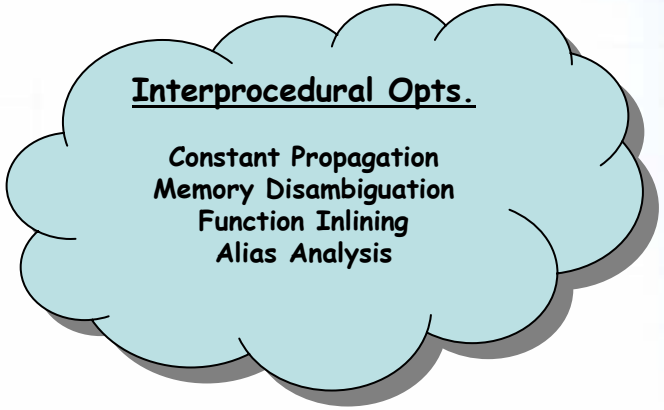
Compiler Optimizations – Dragon Book +





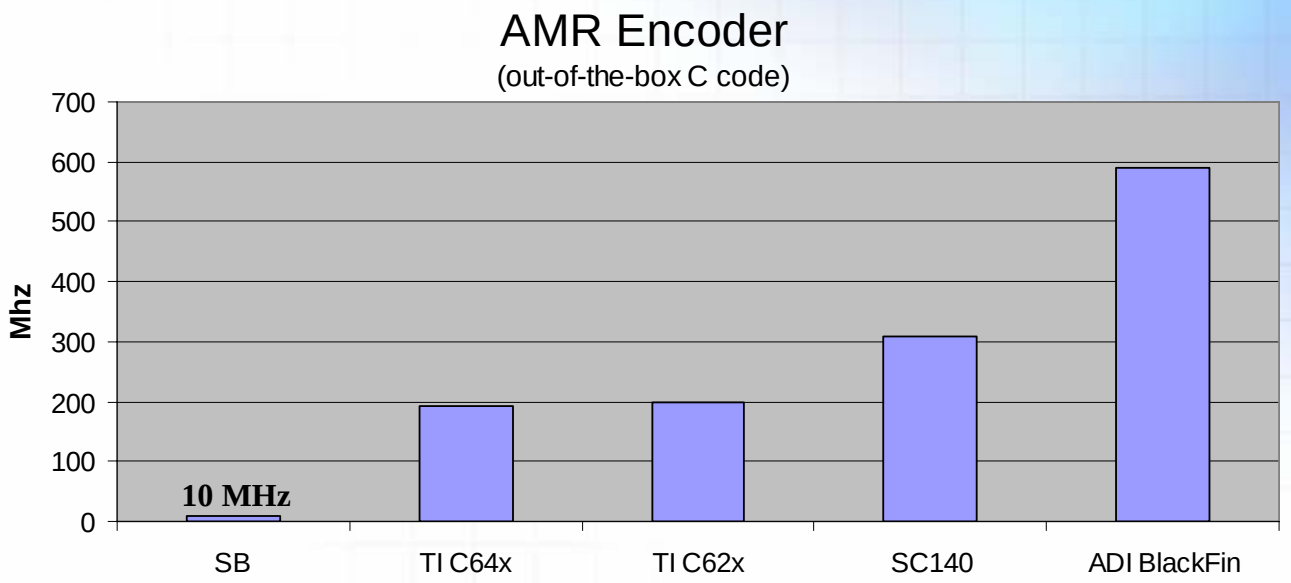






SANDBRIDGE TECHNOLOGIES

Sandblaster AMR Results

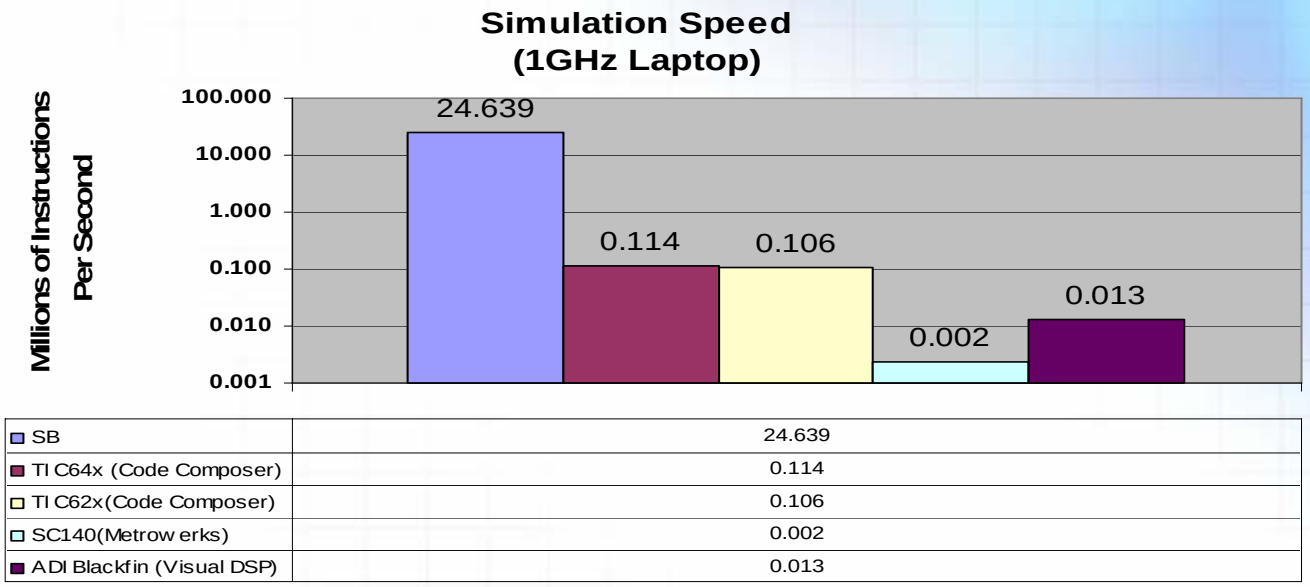


Programmed in C or Java

- Super-computer class compiler
  - Vectorization
  - DSP instruction generation
- Standard Library
  - Printf();
- POSIX pthreads or Java threads
- 50k+ testcases used for validation
  - Industry standards: Plum-Hall, perennial, nullstone

SANDBRIDGE TECHNOLOGIES

Sandbridge AMR Simulation Results



SB	24.639
TI C64x (Code Composer)	0.114
TI C62x(Code Composer)	0.106
SC140(Metrow erks)	0.002
ADI Blackfin (Visual DSP)	0.013

Compiled Simulator

- JIT “Flash” compilation
- Up to 100 MHz on high end x86
- Multi-threaded supported

Up to 4 orders of magnitude faster

- Dramatic development time reduction
- Significant productivity improvement

SANDBRIDGE TECHNOLOGIES

Multithreaded Programming

Automatic Multithreading of DSP Kernels

- Compiler can vectorize and multithread
- Uses pthreads as underlying infrastructure

Multiple threads usage via pthreads library

- POSIX API
- Complete support for thread management, synchronization, and communication
- Thread-safe version of the C library
- Entire coding is done in C

Applications multithreading in Java

- Inherently a multithreaded language

Multithreaded H/W with multithreaded S/W

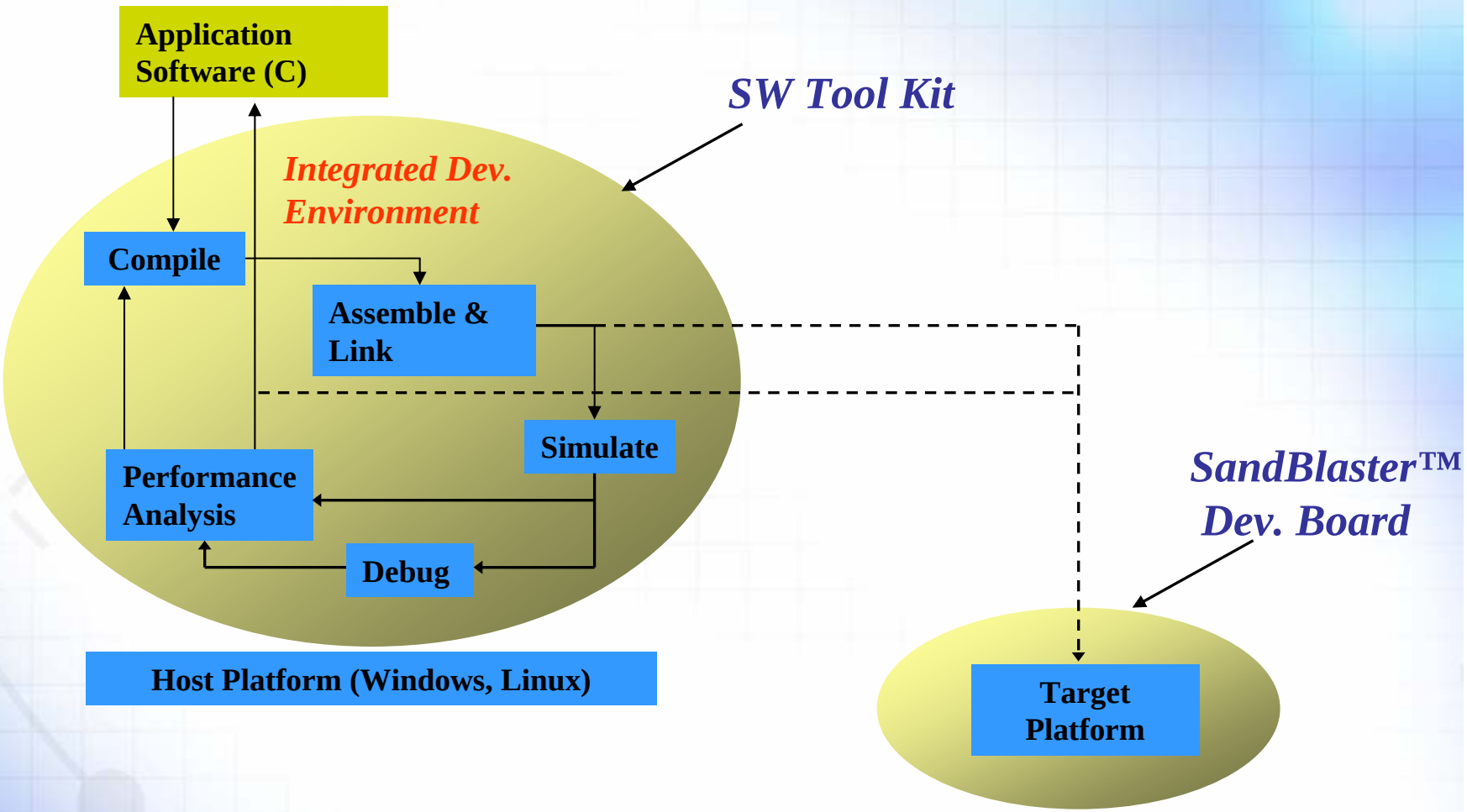
- Automatic mapping of parallelism
- Easy parallel programming methodology

Java Support

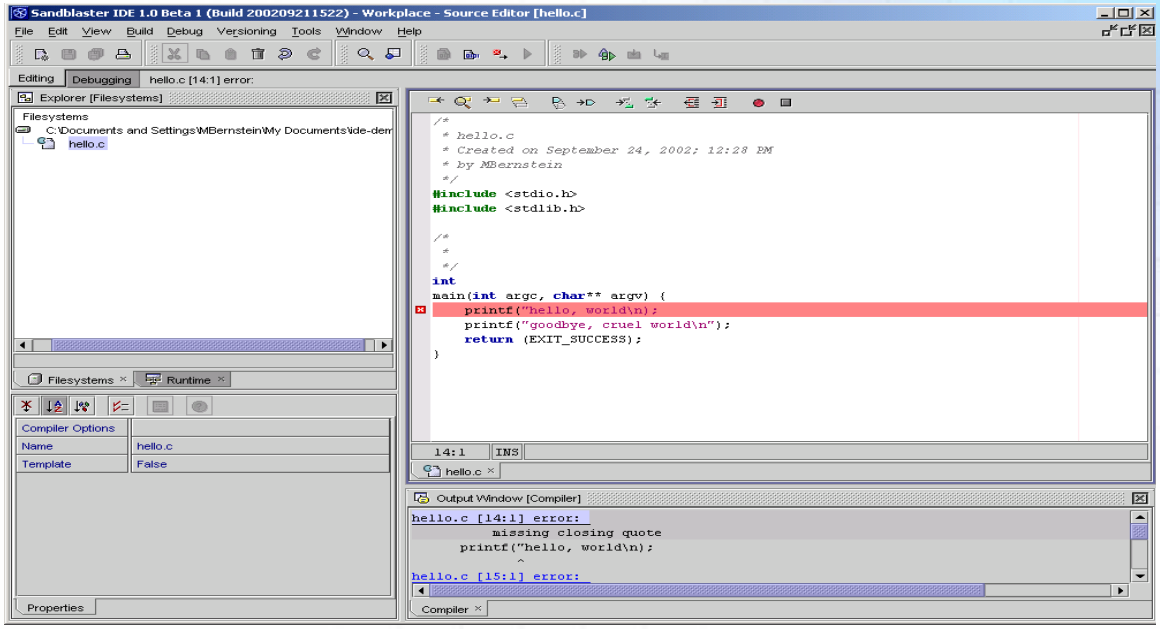
Java J2ME implementation

- KVM 1.0 bytecode engine
- CLDC 1.0
- MIDP 1.0 support provided
  - MIDP 2.0 in process
- Multiple Java threads execute on multiple H/W thread units
  - First known hardware multithreaded KVM
  - Sandblaster tools compile KVM with Java-specific optimizations
  - Java is another application on the Sandblaster processor
  - A java thread is scheduled on any available hw thread unit
    - Dynamic number of hardware thread units may be used
  - Synchronization mechanisms fully supported
  - Multithreaded garbage collection supported

Development Environment



Integrated Development Environment (IDE)



Based on Java open source netbeans

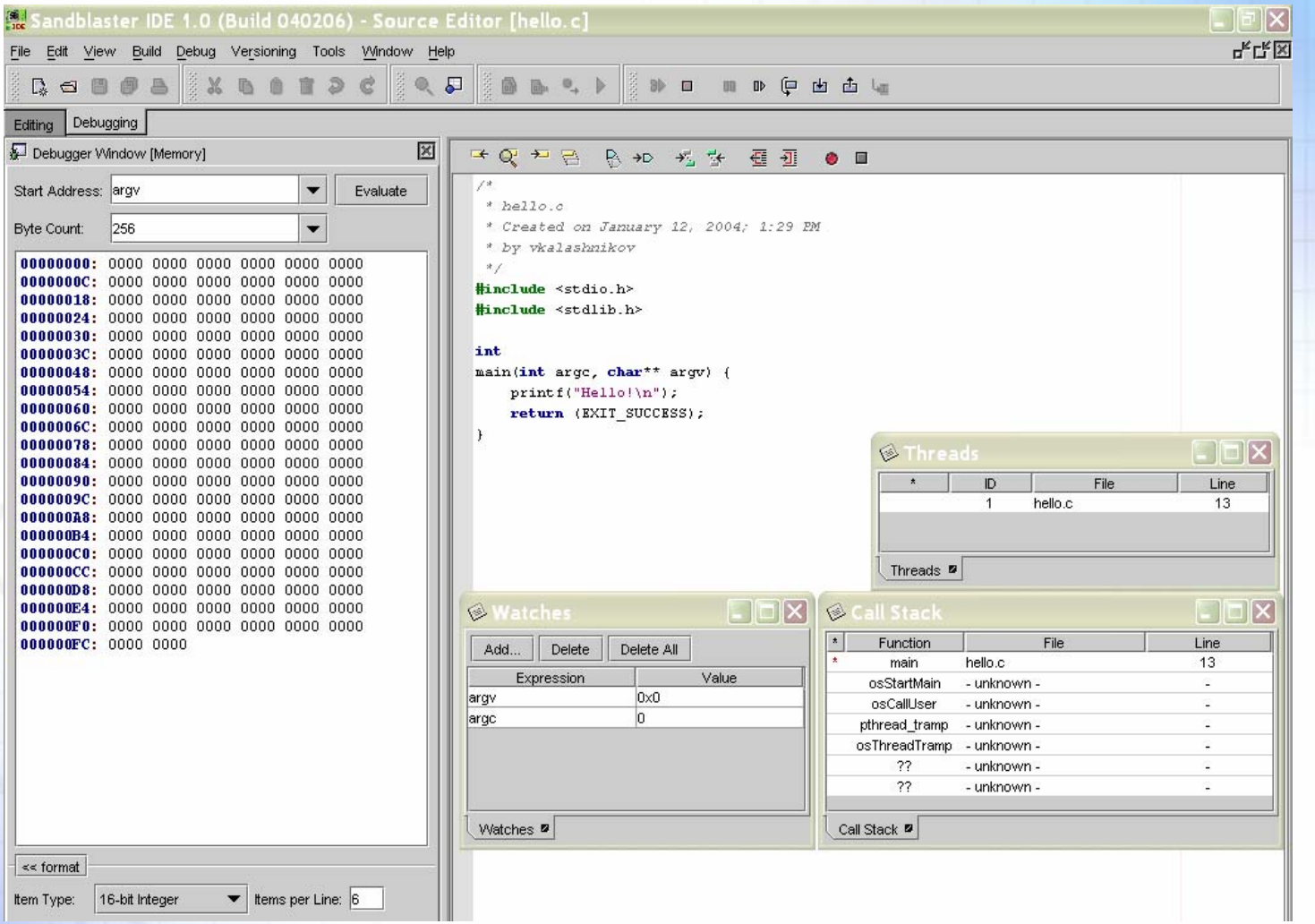
- Enhanced with
  - C compilation and editing tools
  - Source debugger
  - Project management
  - Scripting languages

Automatic Error recognition

Works in multiple languages too!

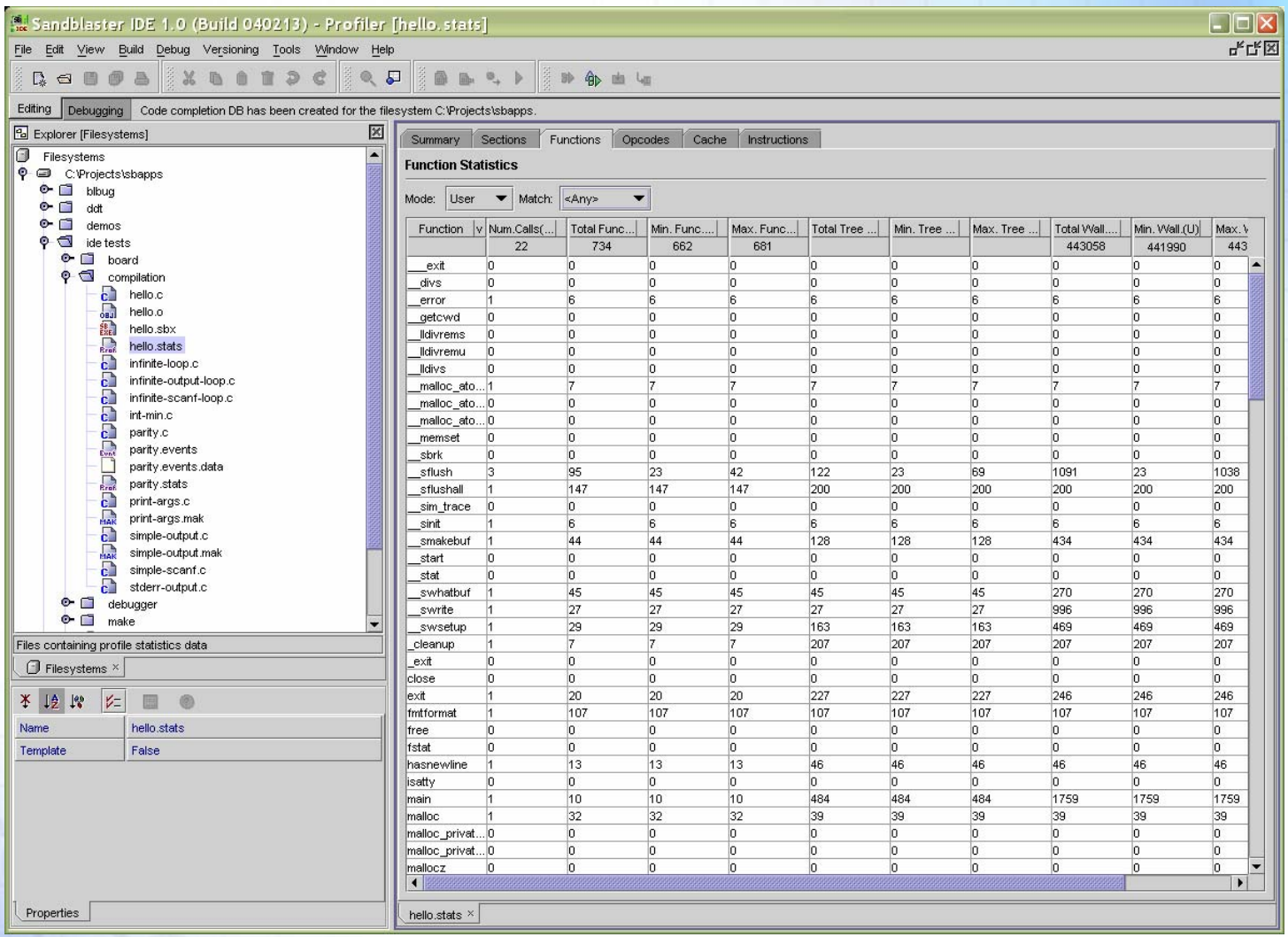
SANDBRIDGE TECHNOLOGIES

Variables, Threads and Memory View in Debugger



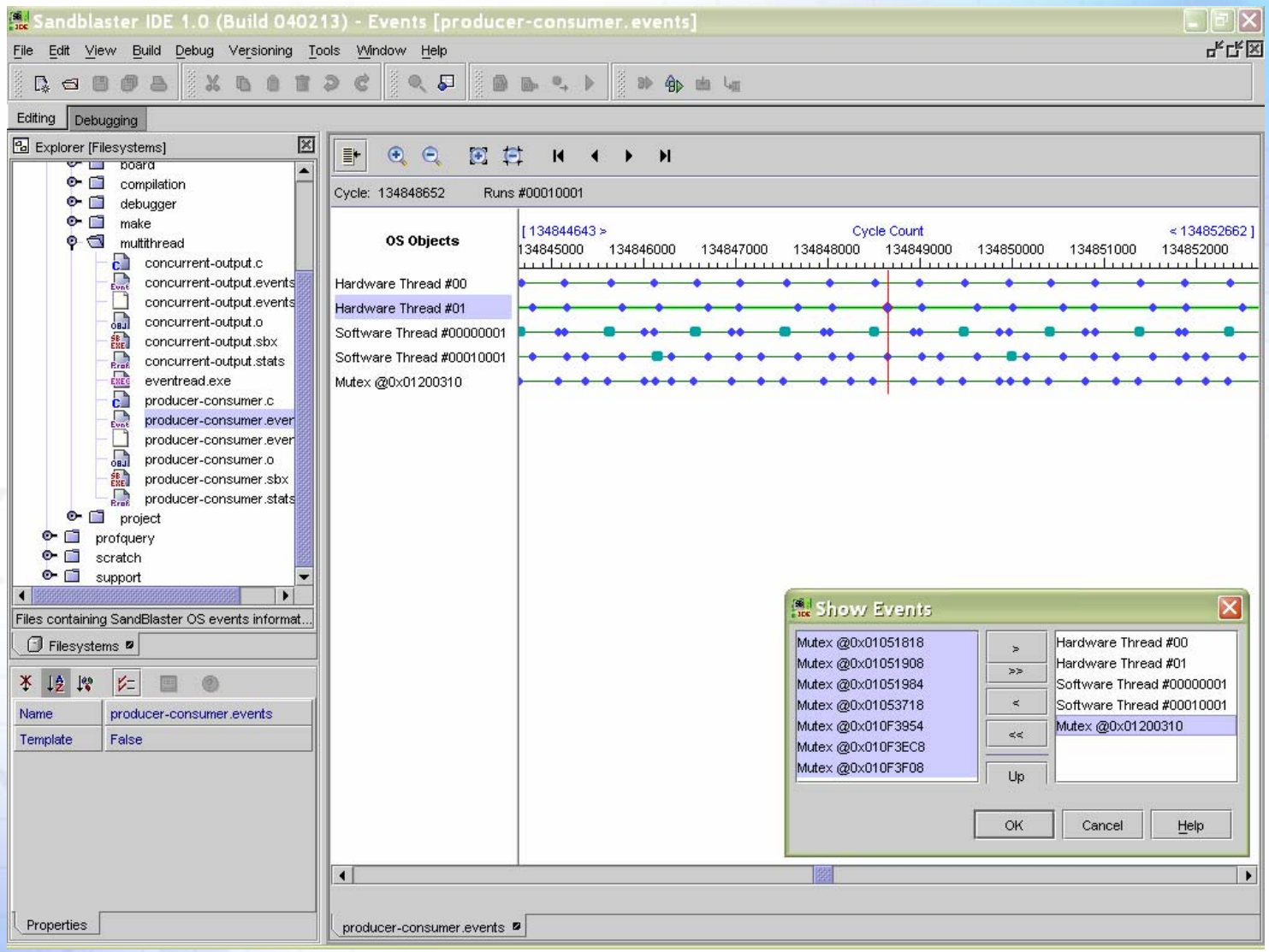
SANDBRIDGE TECHNOLOGIES

Snapshot of Profile Information



SANDBRIDGE TECHNOLOGIES

Event Viewer (GUI)

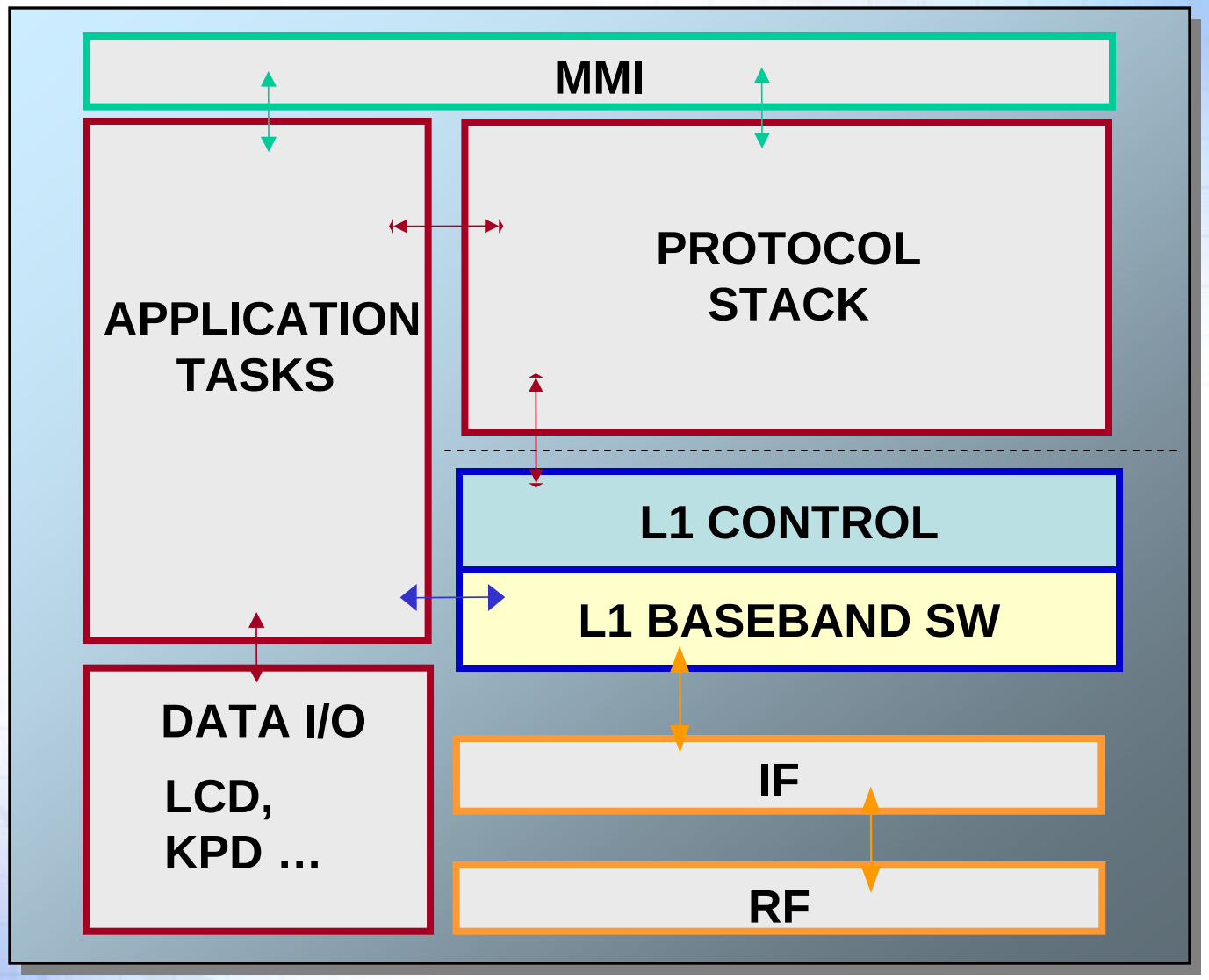


SANDBRIDGE TECHNOLOGIES

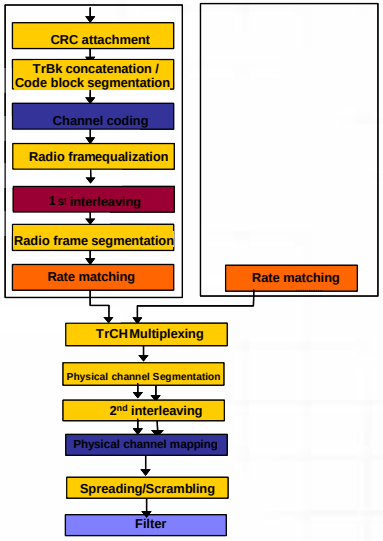
Communications Systems Implementation

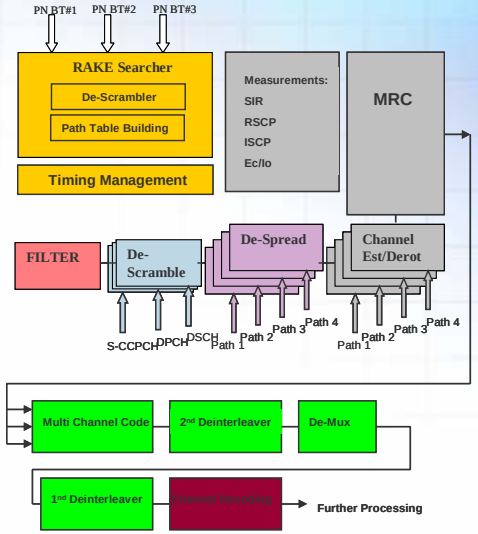
SANDBRIDGE TECHNOLOGIES

Integration



Real-time WCDMA Performance





Real-time chip, bit, and symbol rate processing

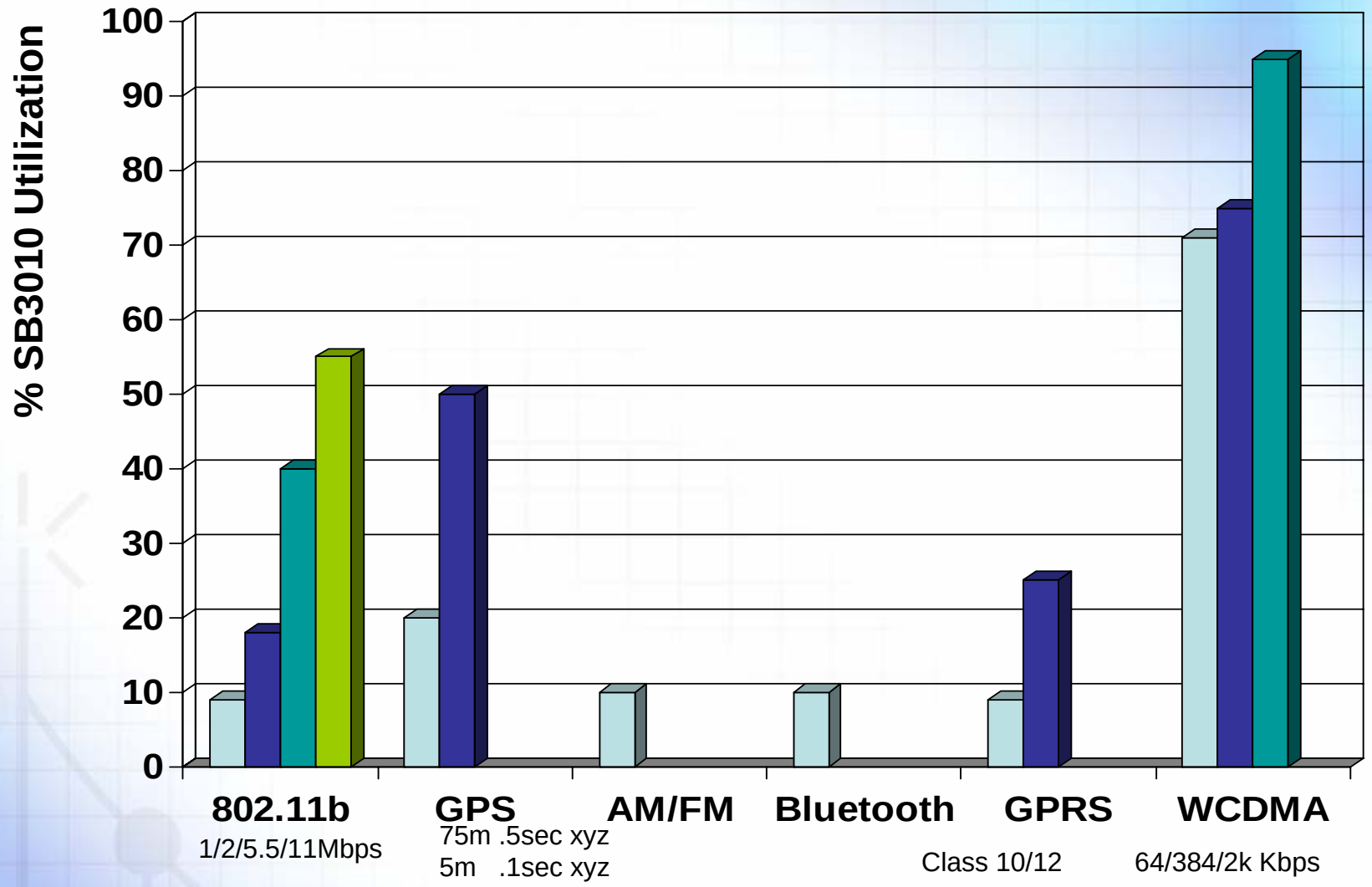
- 1 SB9600 chip for 2Mbps Rx concurrently with 768kbps Tx
- <75% utilization for 384kbps Rx / 384kbps Tx

Includes functions traditionally implemented in H/W

- Turbo Decoder
- Rake Receiver
- Tx/Rx Filters

SANDBRIDGE TECHNOLOGIES

Communications Results



SANDBRIDGE TECHNOLOGIES

Summary

Multithreaded baseband processor

- High-performance and low-power
- DSP, Java, and Control processing

Sophisticated compiler technology

- Automatically generates DSP operations
- Automatically multithreads applications
- Hand coded performance

Reconfigurable Communications Protocols

- WCDMA, GSM, GPRS, etc.
- 802.11b, Bluetooth, etc.

Multimedia capability

- MP3
- MPEG4