Grand Challenges in Embedded Computing

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Mobile Devices get more Features than ever before

WAN
- TD-SCDMA
- W-CDMA
- 1xEV-DO
- 1xEV-DV
- EDGE
- GPRS
- IDEN
- PHS

802.16
802.15
802.11b
a,g,n
BT
IR

LAN/PAN

Broadcast
- DVB-H
- ISDB-T
- DMB
- XMB
- FM

Audio/Video
- MP-3
- AAC+
- WMA
- ATRAC-3
- JPEG
- H.264
- MPEG-2/4

Ease-of-use
- Voice dialing & control
- Handwriting recognition
- SMS dictation

A-GPS Games Encryption

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What is it that we eventually carry with us?

It has a color screen, camera, audio and antenna …
… but all features need high computing performance and ultra low power consumption

- Wireless communication 2G – 2.5G – 3G – WLAN – BT – etc.
  - GSM/IS-95a,b/IS-136/PDC/iDEN – CDMA2k/GPRS/EDGE – FDD/TDD/TD-SCDMA/Jap/WCDMA/CDMA2k-3x– 802.11a,b,g
- Radio broadcast GPS – radio – TV – etc.
  - Location based services/911/tracking services – AM/FM/DAB – Sat./Terr.TV
- Encryption – decryption – media encode – media decode
- Games – speech to text – natural language processing
Compiler Productivity

Design Algorithms → Map to Fixed Point C → Write DSP Specific C → Write DSP Assembly → Compile → Hand Schedule Operations on DSP → Final Product

6-9 Months!

Signal Processing Applications Complexity

10x every 10 years

Lines of C Code:

10E+3

1E+3

1985 1995 2005

September 2005 CODES+ISS
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Parallel Hardware is Required

Thread 0
# Monitoring FCCH&SCH
lu r1,M(r2)
lu r1,M(r2)
cmp cf2,r5,r3
jc cf2,(Synch_off)

Thread 1
# WCDMA Main
Start Thread0
Start Thread1
Start Thread2

Thread 2
# Exit Code
Start Thread33
Start Thread43

Thread 3
# WCDMA Handover Code
ctsr r1,sr2
lu r1,M(r2)
jc cf0,(WCDMA_Mode)

Thread 4
# Pulse shaping Code
lvu vr1,M(r4)
vmacs
vr3,vr1,vr2,wr0
loop lcr0,label(4x)

Thread 5
# FIR Filter
lvu vr1,M(r4)
vmacs
vr3,vr1,vr2,wr0
loop lcr0,label(4x)

Thread 6
# Handover Code
ctsr r1,sr2
lu r1,M(r2)
jc cf0,(UMTS_Mode)

Thread 7
# Monitoring CPICH
lu r1,M(r2)
lu r1,M(r2)
call (De_scrambler)
stu r3,M(r2)

Java Processor

3G Applications Standard
C programmed
Latency hiding architecture

Control Processor
3G, xDSL, 802.11
Control Stacks

System Productivity Advantage
9-12+ months

Key to Low Power Implementation

Sea of Threads

Code & Data Sharing Across Threads

Parallel Hardware is Required

Highly Parallel

Fast Cross Thread Interrupts

C Programmed

Fully Interlocked

Latency hiding architecture
Embedded/DSP vs. General Purpose

**Execution Predictability**
- Required to guarantee real-time constraints
- 1 cycle MAC
- 0-overhead Loop Buffer
- Complex Instructions
  - Multiple Operations Issued
- Harvard Memory Architecture
  - Multiple memory access
- Specialized Addressing Modes
- Operate on Vector Stream Data
- Data-independent Execution
- Fractional Arithmetic
- Pipeline Non-interlocked
  - Shallow Pipeline (3-5 stage)
- Delayed Branch

**Fast But Non-predictable**
- Dynamic Instruction Issue
- Non-deterministic caches
- Multicycle MAC
- Branch Prediction
- RISC Superscalar Instructions
  - Multiple Instructions Issued
- Von Neumann Architecture
  - Split Cache has similar benefit
- Typically Linear Addressing
- Caches Assume Locality
- Data-dependent Execution
  - Dependent upon operands
- Integer Arithmetic
- Pipeline Typically Interlocked
  - Deep Pipeline (5+ stage)
- Multicycle Branch
## Embedded/DSP vs. General Purpose

<table>
<thead>
<tr>
<th>Minimize Worst Cast Execution Time</th>
<th>Minimize Average Execution Time</th>
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Embedded Challenges

Systems become more complex
- Multiple applications
- Competing standards

Software productivity becomes more important
- Assembly optimization not feasible
- Parallel compilers required

Hardware becomes parallel processing
- Multiple concurrent events
- Real-time systems