EVALUATION OF MILITARY WAVEFORM PROCESSING ON A COTS RECONFIGURABLE SDR PROCESSING PLATFORM

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ABSTRACT

Commercial wireless communication terminal manufacturers are beginning to utilize reconfigurable, software defined radio (SDR) digital processing semiconductor devices and standard high level languages to implement power efficient, flexible and adaptable SDR wireless terminals. This study investigates SDR digital baseband processing resource requirements for waveforms anticipated to be employed in future military tactical communication terminals using a state of the practice, commercial, reconfigurable SDR digital processing system-on-a-chip (SOC) device.

Optimized C language waveform code for 802.11, SINCGARS, and Small Unit Operations (SUO) was subjected to operational simulation on the target SoC. Simulation results were used to support estimation of the digital processing loading of military wideband networking waveform (WNW) modes on an SDR digital processing platform. The ease of waveform software porting demonstrated through reuse of legacy C code and the waveform processing performance data presented in this report lead to the conclusion that existing tactical and commercial waveforms can be accommodated in a one or two chip commercial SoC baseband solution configuration based on a device similar to the Sandbridge SDR Baseband processor and it is feasible to consider use of the same technology to support the strenuous class of WNW waveforms envisioned in the JTRS program.

1. INTRODUCTION

Software Defined Radios (SDRs) offer a dynamically reprogrammable method of reusing hardware to implement the physical layer processing of multiple communications systems and applications. SDRs can dynamically change protocols and accept communications systems and applications updates over the air as a service provider requires. Rapid implementation of numerous multimedia applications and multiple wireless communication protocols is easily accomplished on a single programmable platform utilizing an SDR baseband processor.

Furthermore, enhancing the terminal capabilities with new protocols, applications, and functions is achieved through over-the-air dynamic software downloads. This capability reduces product feature support cost, time-to-field, and project risk while increasing R&D and manufacturing productivity.

Recognizing the significance of SDR technology, the Joint Tactical Radio System (JTRS) program supports acquisition and fielding of Software Defined Radios (SDR) that provide interoperable communications through an internationally endorsed open Software Communications Architecture (SCA). The JTRS program plans to replace older, hardware intensive radios with SDRs in which software applications provide waveform generation and processing, encryption, signal processing and other major communications functions.

A Joint Tactical Radio (JTR) set consists of waveform applications, the radio hardware, and associated operating environment, which conform to the Software Communications Architecture (SCA). The JTR set hardware, with the associated SCA operating environment, includes the following component elements:

- Transmitter
- Receiver
- Amplifier
- Modem
- Antenna
- Information Security (INFOSEC) devices
- Hardware-specific interfaces
- Operating System (real-time, POSIX compliant)
- CORBA Common Object Request Broker
- Core Framework software

• Associated adapters/drivers used to interface between the software and hardware
• Software including waveform applications, crypto algorithms, protocols, formats, and routers

The study undertaken in this project directly evaluates the feasibility of SDR implementation of legacy as well as evolving US military waveforms. In this study we focus on the waveform implementation in C only. CORBA and other Core Framework issues are out of scope of this study.

2. SCOPE OF STUDY

The study effort was organized into three "Tasks" as described below.

The Task 1 activity focused on sourcing ANSI C language waveform software for waveforms-of-interest to dismounted military personnel tactical communications (SINCGARS, 802.11b, and SUO wideband waveform) and creating optimized waveform object modules using the SandBlaster optimizing C language compiler. The wireless waveform abstractions of the selected waveforms were then ported to the proprietary SandBlaster™ SDR processor simulator.

The Task 2 effort utilized the cycle-accurate SandBlaster™ SDR digital processor device simulator to perform operational processing of optimized C language wireless waveform software sourced in Task 1 above. As the C language code for each waveform was subjected to simulated wireless terminal operational processing, data was recoded to indicate

- The specific waveform operational mode processed,
- The size of the wireless software code module processed,
- The projected processing resources required for real-time SDR processing of the waveform software.

The Task 3 effort analyzed Task 2 operational simulation results to assess the commercial SDR processing device technology's capacity to meet digital processing requirements of selected JTRS military wireless waveforms.

During Task 3, we examined the results of Task 2 wireless waveform simulation processing and noted the extent to which the simulated commercial SDR digital processing technology appears capable of providing required real-time processing support for military wireless terminal systems utilizing the subject waveforms.

Task 2 simulation results and available public information on the military wideband networking waveform (WNW) were used to support estimation of the digital processing loading of (WNW) modes on an SDR digital processing platform.

As a result of Task 3 analysis, we concluded that the waveform processing performance data presented in this report support the conclusion that existing tactical and commercial waveforms can be accommodated in a one or two chip commercial system-on-a-chip digital baseband processing configuration based on a device similar to the SandBlaster™ SDR processor and it is feasible to consider use of the same technology to support the strenuous class of WNW waveforms envisioned in the JTRS program. It was also observed that use of a SandBlaster-class SDR processor could enable reduction in power-consuming parts of typical military radio terminals by performing both waveform processing and general purpose processing on the SandBlaster – class processing device.

In addition, the ease of waveform software porting demonstrated through reuse of legacy C code and state-of-the-art code optimizing compilers can reduce terminal project development schedules six to nine months.

3. 802.11 PHYSICAL LAYER

IEEE 802.11 is an industry standard set of specifications for WLANs developed by the Institute of Electrical and Electronics Engineers (IEEE). IEEE 802.11 defines the physical layer and media access control (MAC) sub-layer for wireless communications.

At the physical layer, IEEE 802.11 defines both direct sequence spread spectrum (DSSS) and frequency hopping spread spectrum (FHSS) transmissions. At the MAC sub layer, IEEE 802.11 uses the carrier sense multiple access with collision avoidance (CSMA/CA) media access control (MAC) protocol. The 802.11 DSSS physical layer accommodates 2Mbps w/DQPSK or 1Mbps w/DBPSK with 14 channels (11 channels for US). The 802.11 DSSS physical layer transmitter is illustrated in Figure 1 and the receiver in Figure 2.

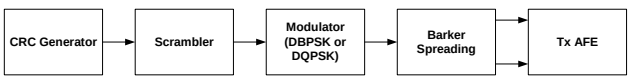

Figure 1 - 802.11 Physical Layer Transmitter

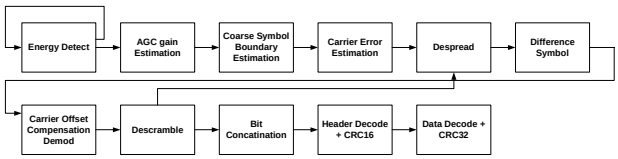

Figure 2 - 802.11 Physical Layer Receiver

As can be seen in the Figures above, the transmitter chain is a direct interpretation of the IEEE 802.11 standards, and the receiver a typical digital receiver with the reverse transmitter processing chain implementation.

The 1Mbps 802.11 physical layer blocks were all implemented in ANSI C. We then optimized the ANSI C code waveform software routines to operate on the SandBlaster SDR processing platform. The optimizations followed ANSI-compliant coding practices stated in the published Sandbridge Technologies coding style guidelines. The C implementation was analyzed using the Sandblaster SDR development tools. The tools included ANSI C optimizing compiler, debugger, cycle accurate simulator and performance analyzer. Based on the performance data obtained, and recognizing that the number of cycles required by the code must run within the 802.11 frame timing constraints to achieve real-time performance, the MHz requirements of the SDR platform were determined. The results are summarized in Table 1.

802.11 Physical Layer	Processing Requirement on 600MHz Sandbridge SDR Baseband Processor (MHz)	Percentage utilization of the 600MHz Sandbridge SDR Baseband Processor
Receiver	244	10%
Transmitter	78	3%

Table 1 - 802.11 Receiver/Transmitter MHz Analysis

As noted above, the software implementation of the 1Mbps 802.11 physical layer consumes less than 15% of the performance bandwidth of the 4-core 600MHz Sandbridge SDR Baseband Processor. It is therefore concluded that not only real time performance of the 802.11 physical layer processing is readily achieved by it software implementation on the Sandbridge SDR Baseband Processor, but also 85% of the processor is available to run other waveforms or applications concurrently.

4. SINCGARS PROCESSING REQUIREMENTS

The Single Channel Ground and Airborne Radio System (SINCGARS) provides commanders with a highly reliable, secure, easily maintained Combat Net Radio (CNR) that has both voice and data handling capability in support of command and control operations. SINCGARS, with the Internet Controller, provides the communications link for Task Force XXI. SINCGARS configurations include man pack, vehicular (both low and high power), and airborne models. SINCGARS is a family of VHF-FM combat net radios which provides the primary means of command and control for Infantry, Armor and Artillery Units. SINCGARS is designed on a modular basis to achieve maximum commonality among the various ground and airborne system configurations. A common Receiver Transmitter (RT) is used in the man pack and all vehicular configurations. SINCGARS family of radios has the capability to transmit and receive voice, tactical data and record traffic messages and is consistent with NATO interoperability requirements. The system operates on any of the 2320 channels between 30-88 megahertz and is designed to survive in a nuclear environment. [10]

Based on algorithmic analyses performed on both Fixed Frequency (FF) and frequency Hopping (FH) modes of the SINCGARS waveforms, it became apparent that the FH mode is more computationally intensive than the FF mode. Therefore the performance numbers extracted from the FH mode set an upper bound on the MHz requirements on the Sandblaster SDR baseband processor.

We acquired access to thirty five (35) ANSI C code software routines to perform acquisition processing of SINCGARS Frequency Hopping mode waveforms on the SandBlaster SDR processing platform.

We then optimized the ANSI C code waveform software routines to operate on the SandBlaster SDR processing platform. The optimizations followed ANSI-compliant coding practices stated in the published Sandbridge Technologies coding style guidelines. The results of the simulation of the FH mode of SINCGARS are tabulated in Table 2.

It is noteworthy that out of the entire processing requirements of SINCGARS, about 60% is concentrated in the pre- and post-detect phases, and the remaining 40% in the rest of the algorithms and procedures.

The "FH bit sync acquisition phase 1", the initial correlation on an FH received signal and "FH bit sync acquisition phase 2", the fine correlation. The initial correlation is a rough initial correlation, and the fine correlation does “fine/full” resolution correlations centered on the location determined by the coarse correlation.

This number of cycles consumed by these correlations was averaged over the total number of cycles in the simulation. The post detect process is running in "background" on candidates found by the pre-detect routine running in foreground.

Block	Performance Requirement (MHz)	Percentage utilization of the 600MHz Sandbridge SDR Baseband Processor
Pre-Detect	94.7	3.95%
Post-Detect	32.2	1.34%
Other	84.6	3.53%
Total	211.5	8.81%

Table 2 - SINCGARS MHz Analysis

5. SMALL UNIT OPERATION (SUO) ACQUISITION CHAIN PROCESSING REQUIREMENTS

The continued development and availability of a software defined family of radios, based on a common open architectural framework and a family of platform-interchangeable waveform software "applications" is proposed as an important enabler for many of the technological elements of the FCS. Accordingly, programs like ACN, FCS-C, CECOM's MOSAIC ATD, and SUO SAS all must maintain their vision of a family of JTRS target platforms, and continue the development of more than just the set of necessary interchangeable legacy waveforms, but also the development and implementation of a family of new enabling wideband multiple access waveforms designed for specific JTRS applications (e.g. airborne advantaged nodes). [8] As the high bit rate waveform component of this study, we acquired access to the SUO waveform implementation in fixed point ANSI C. We then proceeded to optimize ANSI C code SUO Acquisition Chain software (9 routines) to perform physical layer processing of code SUO Acquisition Chain software on the SandBlaster SDR processing platform. The optimizations were ANSI compliant coding practices stated in the Sandbridge coding style guidelines.

The results are tabulated in Table 3.

Chip Rate (Mcps)	Total MHz Requirements	Percentage utilization of the 600MHz Sandbridge SDR Baseband Processor
32	8,279	345%
16	4,139	172%
8	2,070	86%
4	1,035	43%

Table 3 – SUO Acquisition Chain MHz Analysis

Based on the data collected in this part of the study, it can be seen that 4 and 8 Mcps (Mega chips per Second) rates of the SUO Acquisition chain can run in real time on a single Sandbridge SDR Baseband Processor.

6. CONCLUSIONS

In this SDR study, a number of representative waveforms were selected to be benchmarked for the feasibility analysis of their SDR implementation on a Sandbridge SandBlaster-class SDR Baseband Processor. These waveforms ranged from narrow bandwidth waveforms such as SINCGARS to wide bandwidth, high computation waveforms such as SUO.

Through the study, the following points were demonstrated:

1. Given ANSI C implementations of baseband processing waveforms, deployment of these waveform on the SandBlaster™ processor is a relatively routine, time-efficient process

2. With the ANSI C implementation of a baseband processing waveform, very accurate data on the performance on the SandBlaster™ processor can be obtained, through the Sandbridge cycle accurate simulator, which is an integral component of the Sandbridge Software Development Tools. Use of such a simulator tool eliminates the need for the typical terminal development delay associated with waiting for hardware to become available, in order to run waveform code on the target hardware platform.

3. The architecture of the SandBlaster™ processor, along with its vector processing capabilities, allows for very efficient processing of waveform and application code output of the Sandbridge C compiler. The compiled code is equivalent in performance to the hand-coded assembly code

The conclusions drawn from the reported study, as evidenced in the tables presented in this report, are that a pure ANSI C language software implementation of military waveforms on the SandBlaster-class, reconfigurable SDR processor is feasible. The processing requirements of the studied waveforms fall within that of a one or two chip SandBlaster-class solution.

It is recommended that additional study be performed to assess the potential enhanced wideband waveform SDR processing performance that may be realized through waveform software algorithmic enhancements and potential processing platform feature/architecture enhancements.

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