SANDBRIDGE

Multithreaded Processor for Software Defined Radio

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SANDBRIDGE TECHNOLOGIES

Agenda

Motivation for SDR

Multithreaded SDR Processor

Software Development Tools

- Compiler
- Simulator
- IDE

Communications System Implementation

- 2Mbps WCDMA
- 802.11b

The Challenges of an Industry

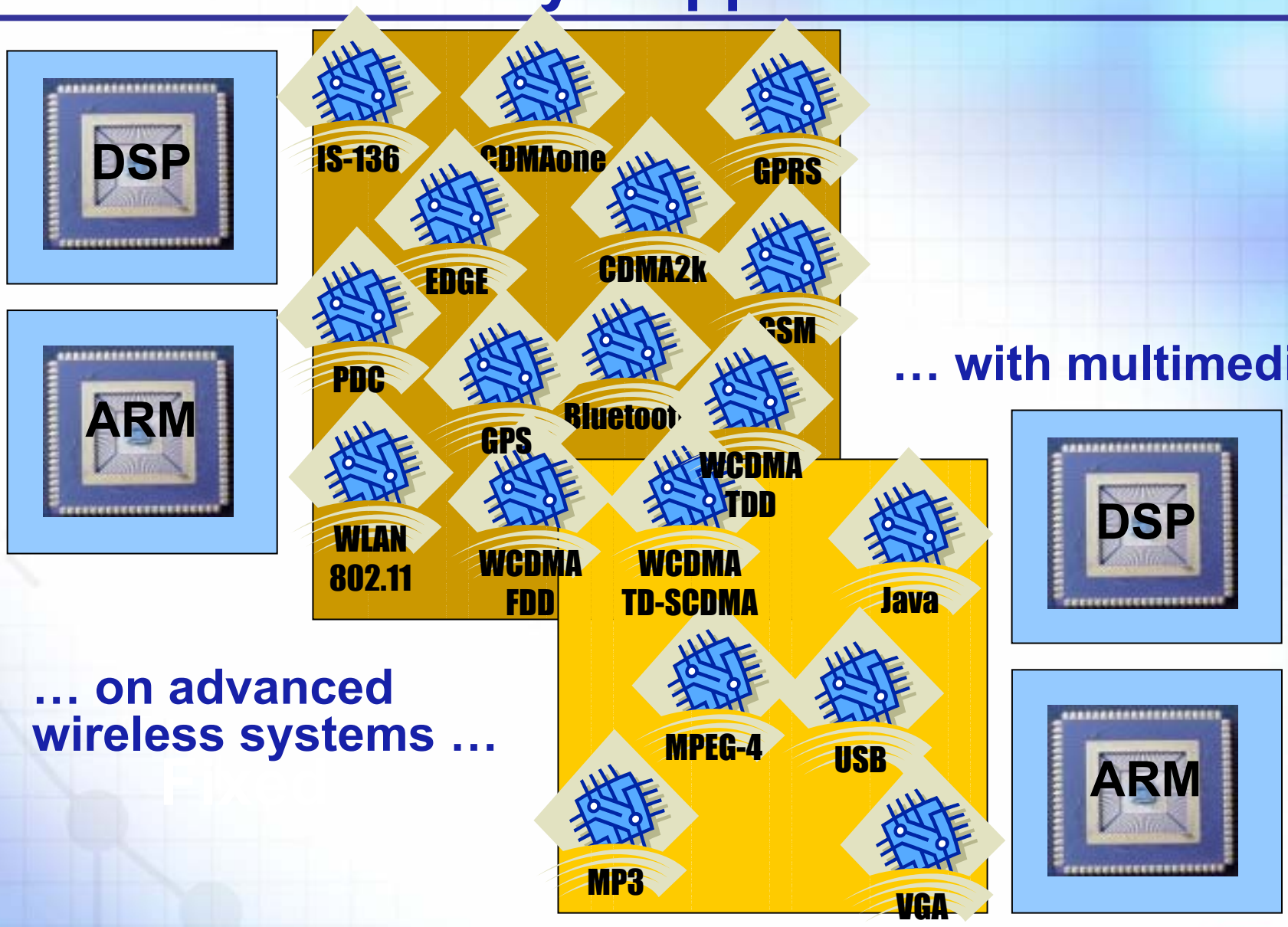
Cost

- 3G is >10x more complex than 2G
  - but cost should be same, or even less
- Convergence phone 2x complexity
  - WLAN, 2G, and 2.5G integration
  - Traditionally implemented in HW
- Moore's law reduces cost 50% every 18 months
  - 6 years until the wireless multimedia is a real consumer market

Time-to-market

- GPRS terminals were late
  - OEMs had to wait until bug free SoCs were available
- 3G terminals will be late
  - OEMs have to wait until bug free SoCs with 'reasonable' power consumption are available

A Whole Industry's approach failed …



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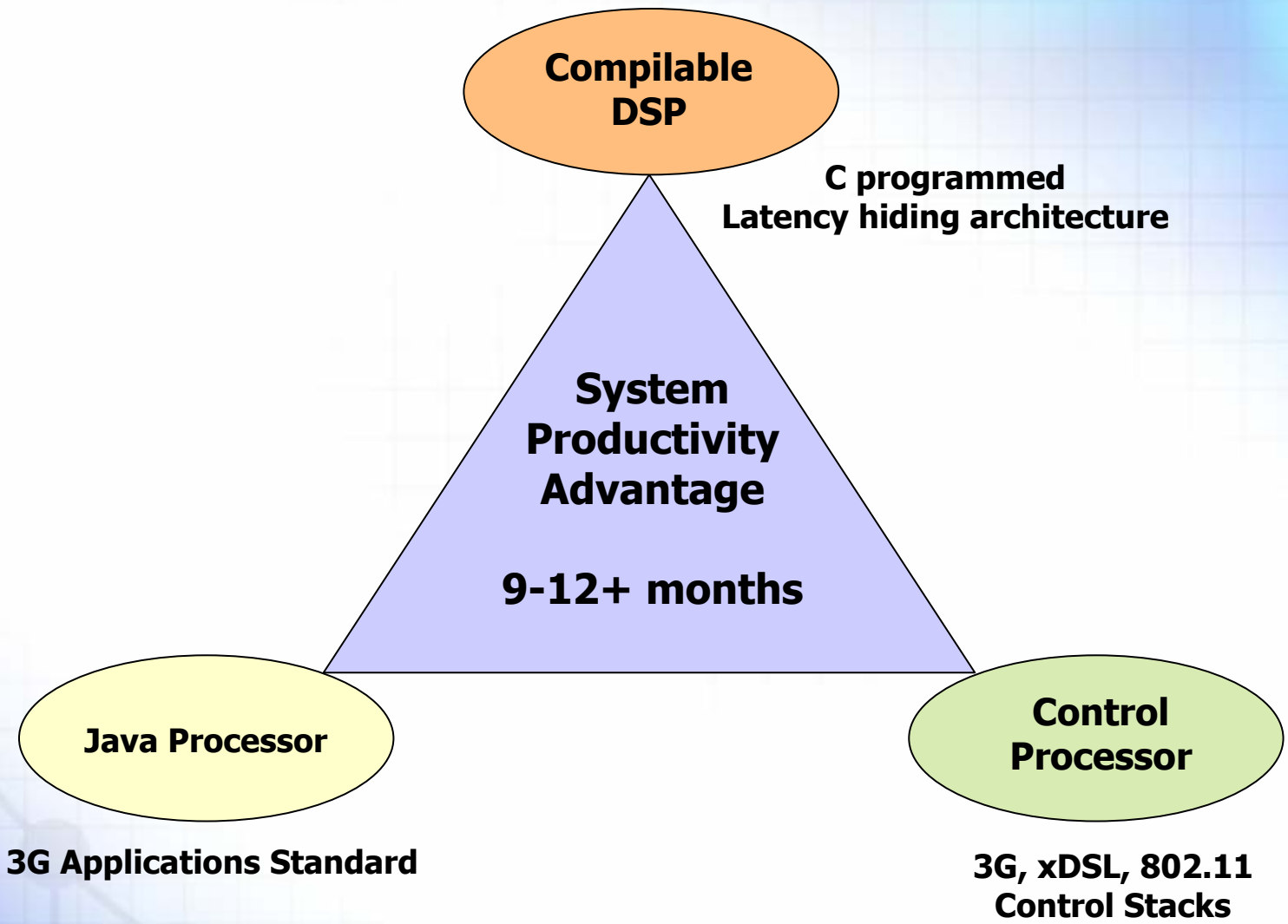
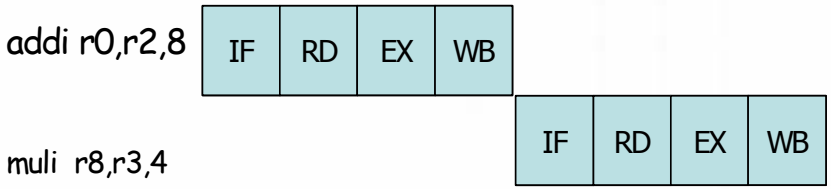
Sandblaster™ Architecture Performs

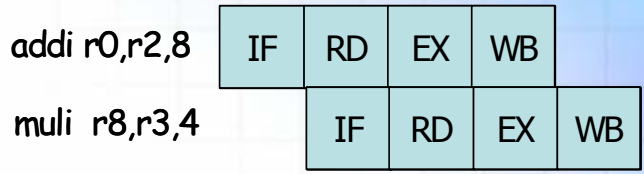


Processor Execution Models

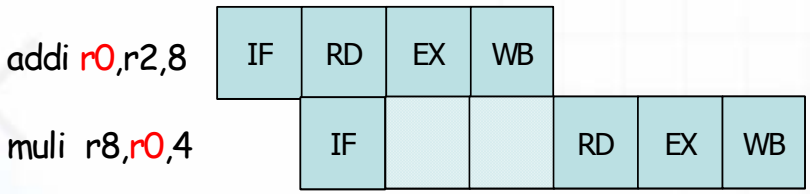
Monolithic Processor



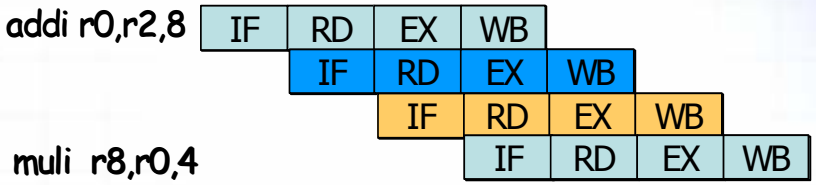
Pipelined Processor



Pipelined Processor Stalls



Multithreaded Processor



Multithreaded Architecture

Key to Low Power Implementation

Code&Data Sharing Across Threads

Sea of Threads

Hardware Scheduled

Highly Parallel

Fully Interlocked

Fast Cross Thread Interrupts

C Programmed

Thread 0

```
# Monitoring FCCH&SCH
lu  r1,M(r2)
lu  r1,M(r2)
add r2,r3,r4
cmp cf2,r5,r3
jc  cf2,(Synch_off)
```

Thread 1

```
# WCDMA Main
Start Thread0
Start Thread1
Start Thread2

Start Thread13
Start Thread14
loop lc1,0xf0
```

Thread 2

```
# Exit Code
.
Start Thread33
.
.
Start Thread24
```

Thread 3

```
# WCDMA Handover Code

ctsr r1,sr2
lu r1,M(r2)
.
jc cf0,(WCDMA_Mode)
```

Thread 4

```
# Pulse shaping Code

lvuvr1,M(r4)
vmacs vr3,vr1,vr2,wr0
loop lcr0,label(4x)
```

Thread 5

```
# FIR Filter

lvu vr1,M(r4)
vmacs
   vr3,vr1,vr2,wr0
loop lcr0,label(4x)
```

Thread 6

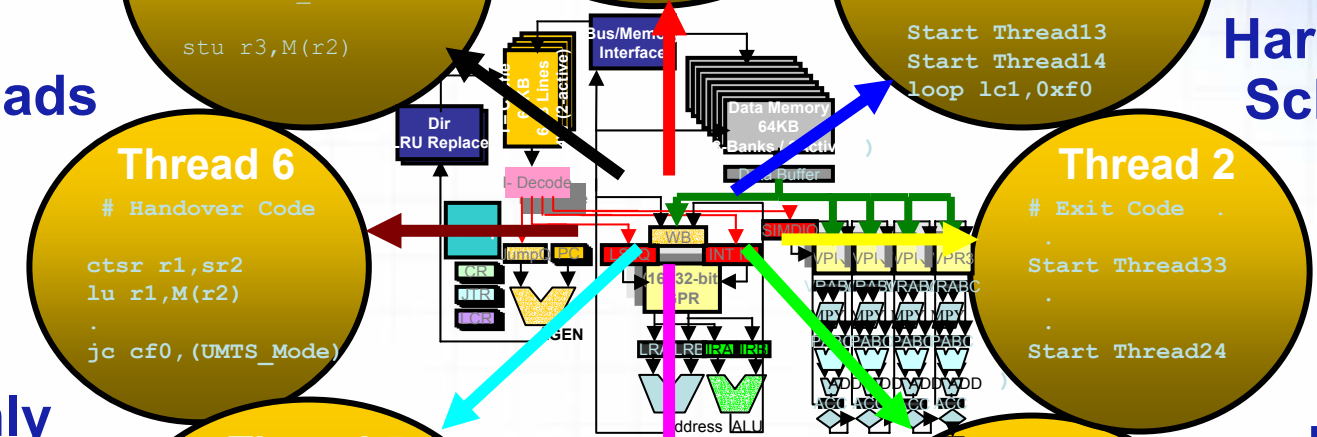
```
# Handover Code

ctsr r1,sr2
lu r1,M(r2)
.
jc cf0,(UMTS_Mode)
```

Thread 7

```
# Monitoring CPICH
lu r1,M(r2)
lu r1,M(r2)
call (De_scrambler)

stu r3,M(r2)
```



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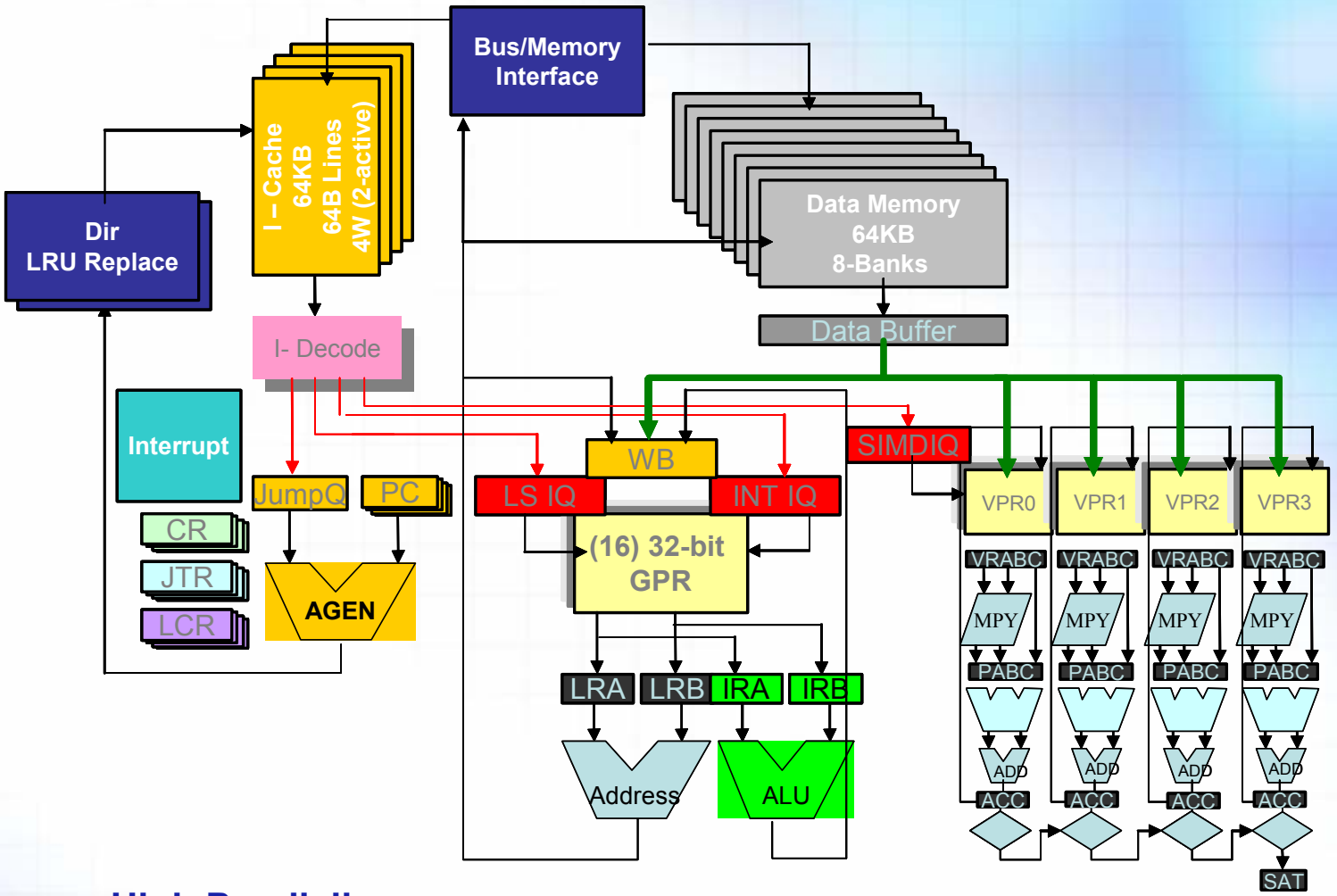
Multithreaded Baseband Processor



High Parallelism

- Vector / SIMD data parallelism
- Multiple instruction issue
- Thread-level parallelism

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Performance

Peak

- 3 compound operations/cycle
- >20 RISC-ops/cycle
- 4 MACS/cycle (MAC-SAT-ADD-SAT)

Example

```
L0: lvu %vr0,%r3,8
||  vmulreds %ac0,%vr0,%vr0,%ac0
||  loop %lc0,L0
```

- >20 operations packed into a 64-bit compound ISA
- VLIW machines may require 512+ bits

20 tap FIR

- 3.63 taps/cycle sustained

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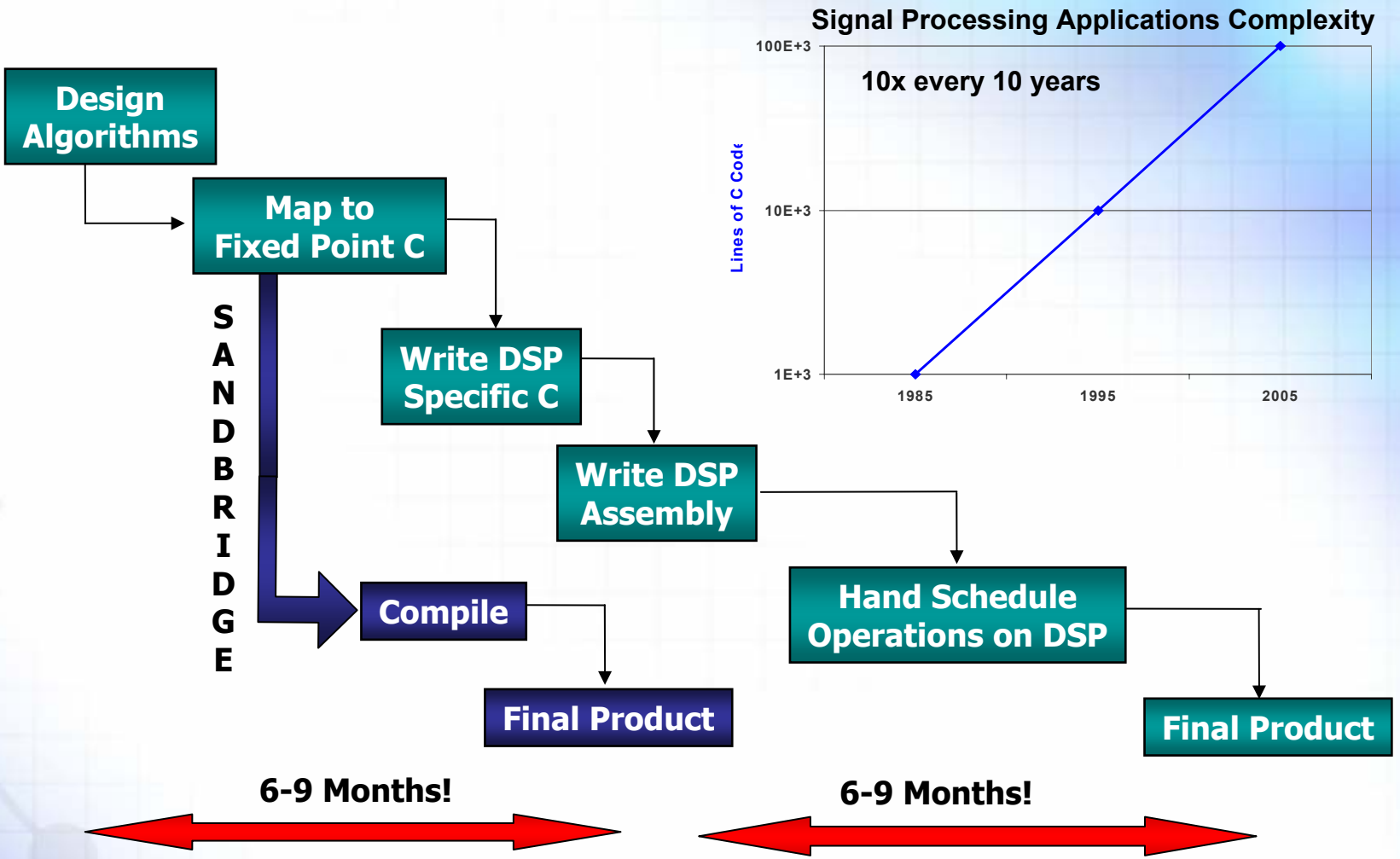
Compiler Productivity



Sandblaster™ Provides Dramatic Improvement

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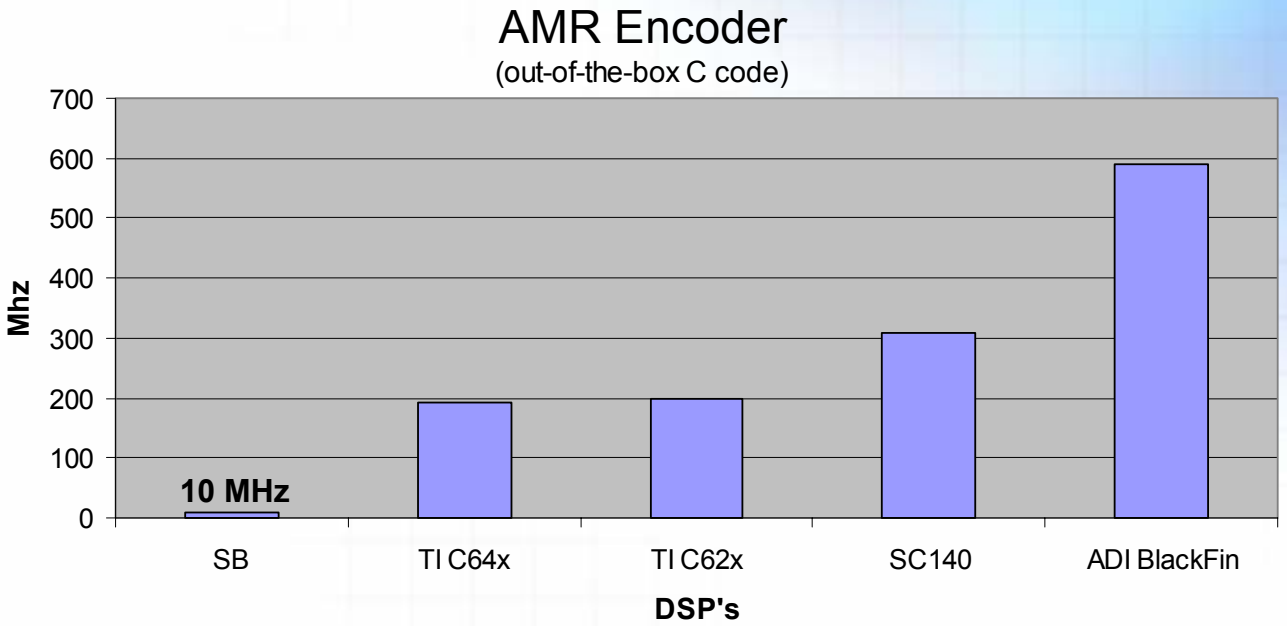
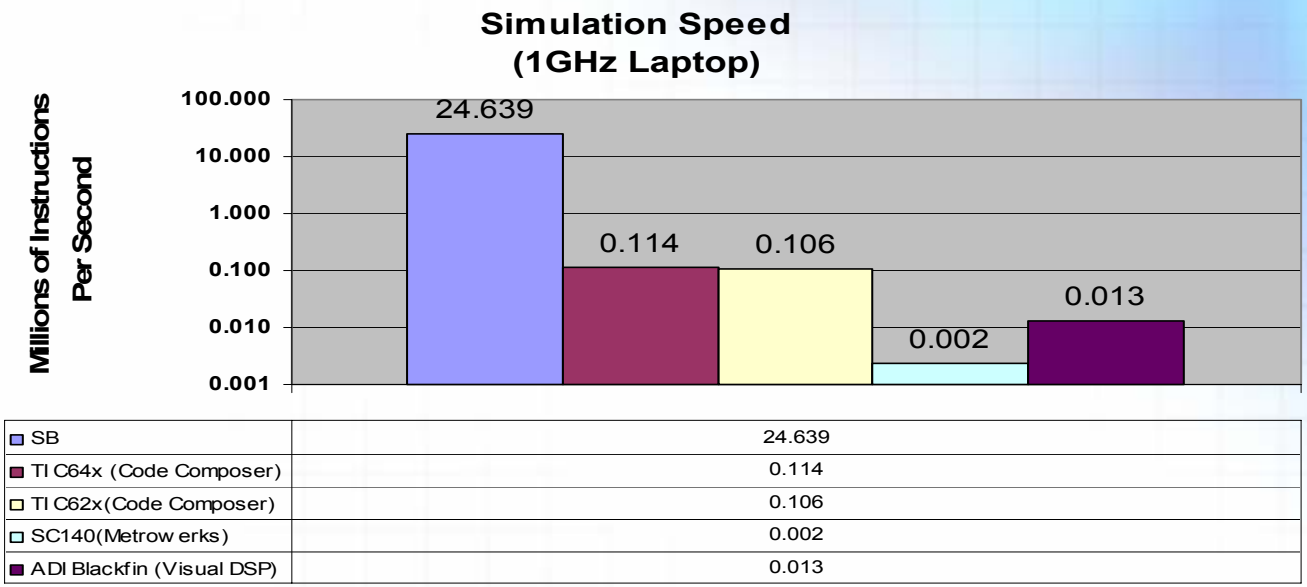
Compiler



Programmed in C or Java

- **Super-computer class compiler**
  - Vectorization
  - DSP instruction generation
- **Standard Library**
  - Printf();
- **POSIX pthreads or Java threads**
- **50k+ testcases used for validation**
  - Industry standards: Plum-Hall, perennial, nullstone

Simulation Software



SB	24.639
TI C64x (Code Composer)	0.114
TI C62x(Code Composer)	0.106
SC140(Metrow erks)	0.002
ADI Blackfin (Visual DSP)	0.013

Compiled Simulator

- JIT "Flash" compilation
- Up to 100 MHz on high end x86
- Multi-threaded supported

Up to 4 orders of magnitude faster

- Dramatic development time reduction
- Significant productivity improvement

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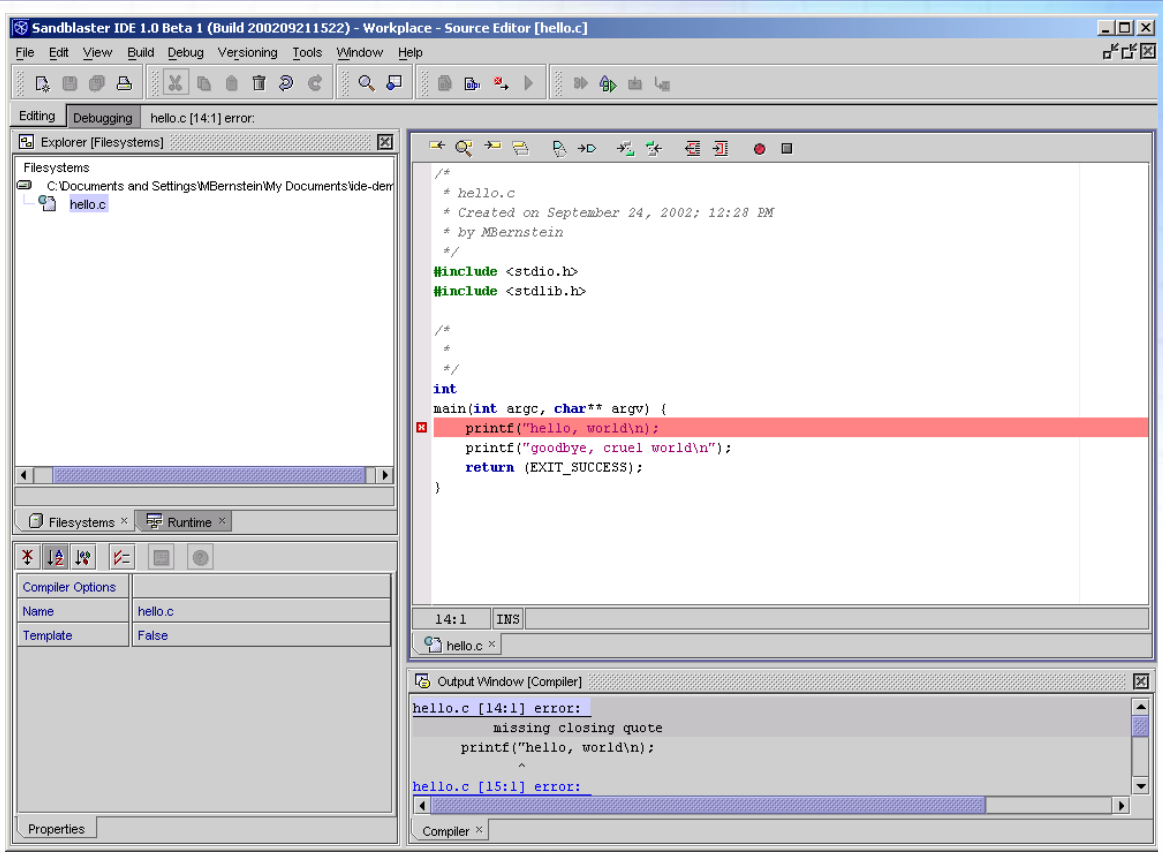
Context sensitive IDE



IDE based on open source netbeans

- Common Java/C programming environment
- Integrated debugging
- Transparent HW / Simulation environment
- Works in multiple languages

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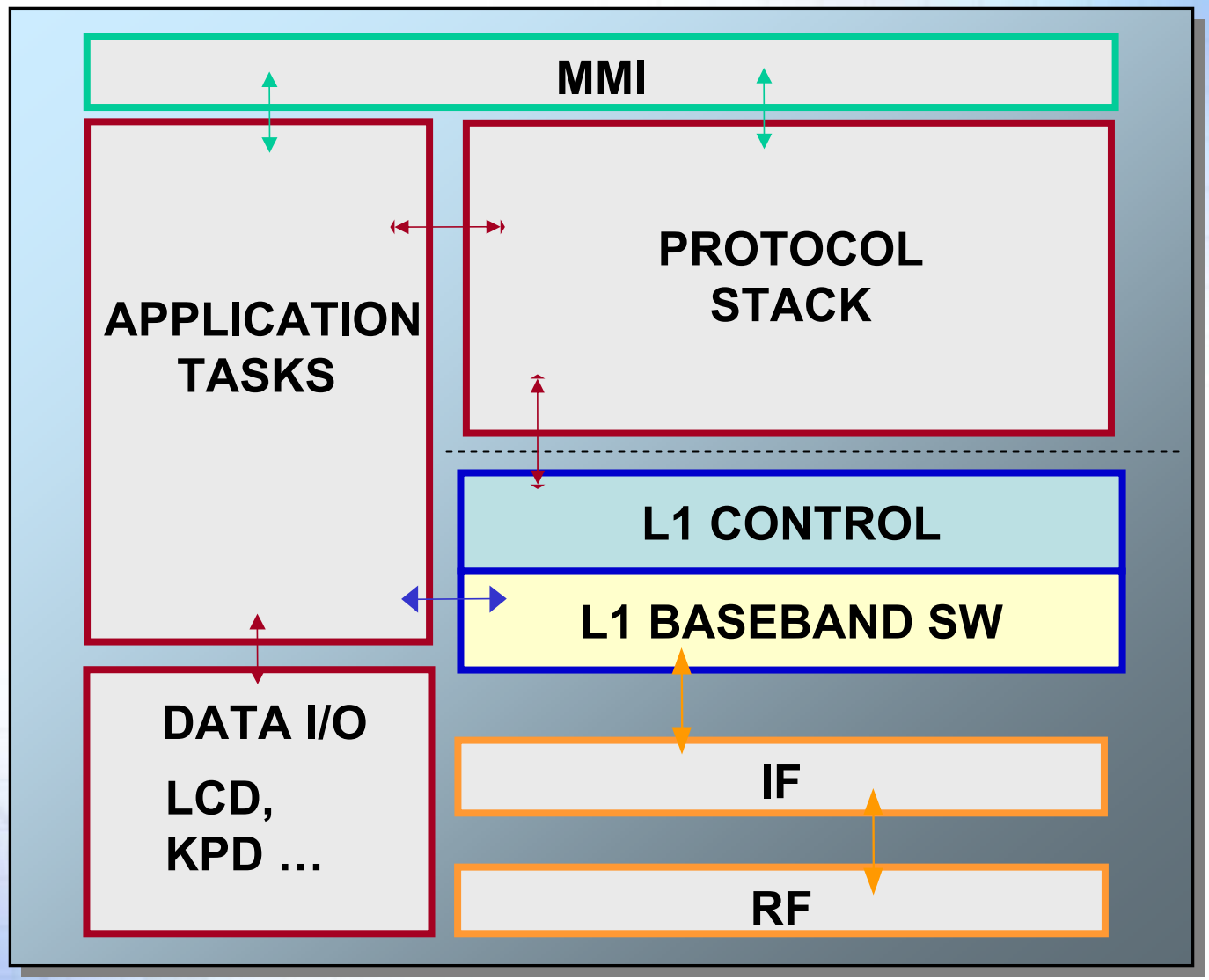
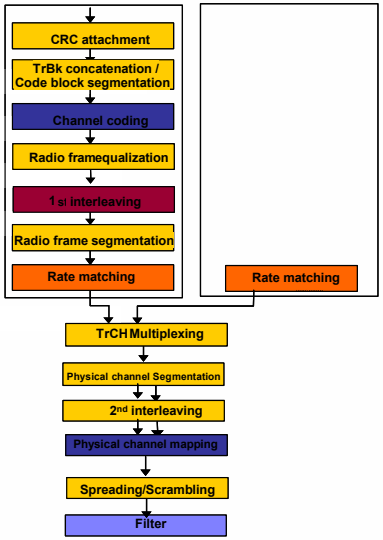
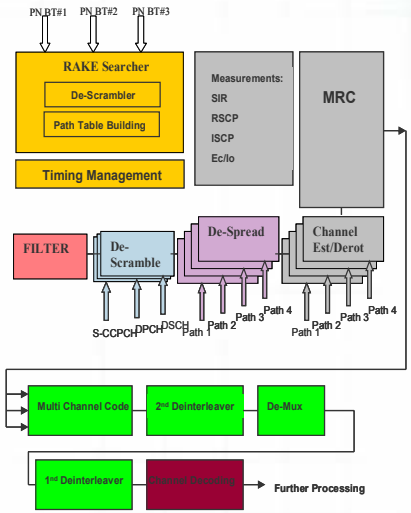
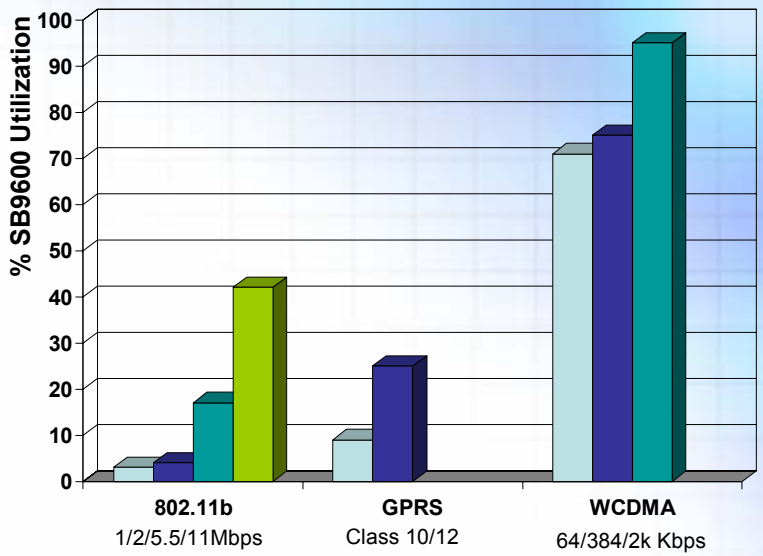
Integration



Real-time Baseband Performance







Real-time chip, bit, and symbol rate processing

- 1 SB9600 chip for 2Mbps Rx concurrently with 768kbps Tx
- <75% utilization for 384kbps Rx / 384kbps Tx

Includes functions traditionally implemented in H/W

- Turbo Decoder
- Rake Receiver
- Tx/Rx Filters

Concurrent performance on 802.11B and GPRS

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Summary

Multithreaded baseband processor

- multi-threaded
- high-performance and low-power

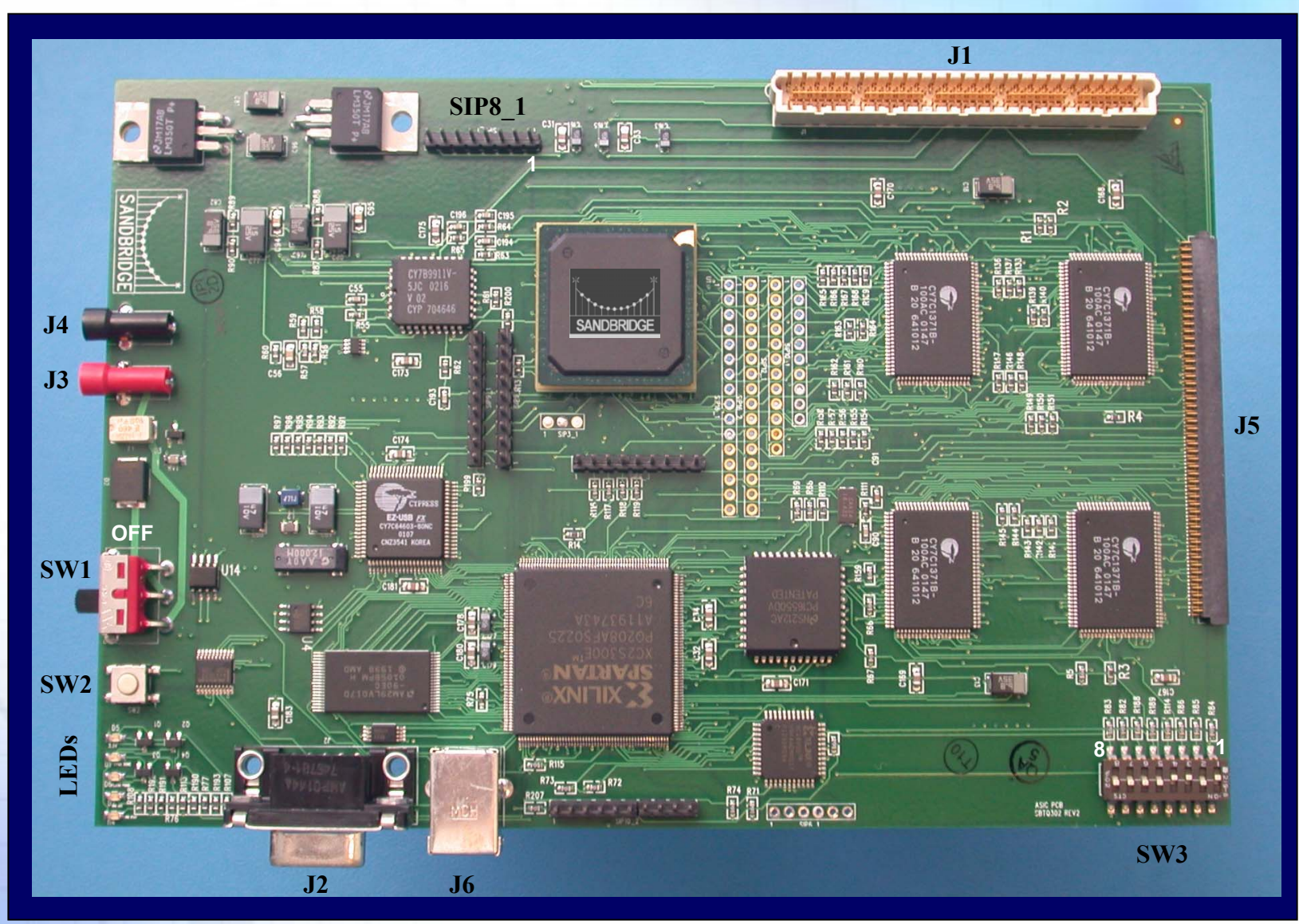
Sophisticated compiler technology

- automatically generates DSP operations
- near-assembly language performance

Reconfigurable Communications Protocols

- WCDMA
- GSM, GPRS
- 802.11
- Bluetooth
- GPS

Populated Multimode Baseband Card



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